MOTOROLA

MC10109

MECL 10K

DUAL 4-5-INPUT "OR/NOR" GATE

The MC10109 is a dual 4-5 input OR/NOR gate.

P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t_r, t_f = 2.0 ns typ (20%–80%)

DUAL 4-5-INPUT "OR/NOR" GATE

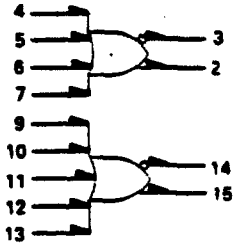
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

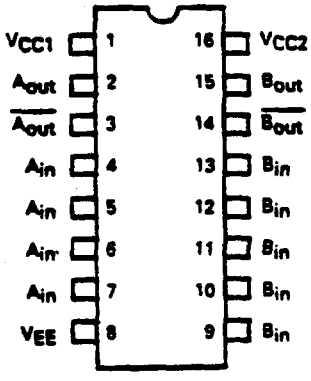
3

LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-31.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10109 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS BELOW: $V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	15	–	11	14	–	15	mAdc	–		–		8	1,16
Input Current	I_{inH}	4		425	–	–	265	–	265	μAdc	4	–			8	1,16
	I_{inL}	4	0.5	–	0.5	–	–	0.3		μAdc	–	4			8	1,16
High Output Voltage	V_{OH}	2	−1.050	−0.890	−0.980		−0.810	−0.880	−0.700	Vdc	4	–			8	1,16
		3	−1.050	−0.880	−0.980	–	−0.810	−0.880	−0.700	Vdc	–	–			8	1,16
Low Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	–			8	1,16
		3	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	4				8	1,16
High Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980			−0.910		Vdc	–	–	4	–	8	1,16
		3	−1.080		−0.980	–		−0.910		Vdc	–	–	–	4	8	1,16
Low Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc		–	–	4	8	1,16
		3		−1.655	–	–	−1.630		−1.595	Vdc		–	4	–	8	1,16
Switching Times (50-ohm load)													Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	t_{d+2+}	2	1.0	3.7	1.0	2.0	2.9	1.0	3.7	ns			4	2	8	1,16
	t_{d-2-}	2										–		2		
	t_{d+3-}	3									–	–		3		
	t_{d-3+}	3										–		3		
Rise Time (20 to 80%)	t_{2+}	2	1.1	4.0	1.1		3.3	1.1	4.0		–	–		2		
	t_{3+}	3									–	–		3		
Fall Time (20 to 80%)	t_{2-}	2									–	–		2		
	t_{3-}	3									–	–		3		

MOTOROLA

MC10124

QUAD TTL TO MECL TRANSLATOR

The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and −5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

P_D	= 380 mW typ/pkg (No Load)
t_{pd}	= 3.5 ns typ (+ 1.5 Vdc in to 50% out)
t_r, t_f	= 2.5 ns typ (20%–80%)

MECL 10K

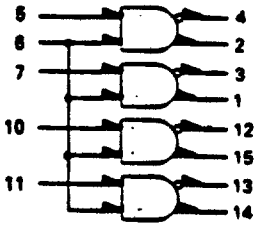
QUAD TTL TO MECL TRANSLATOR

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

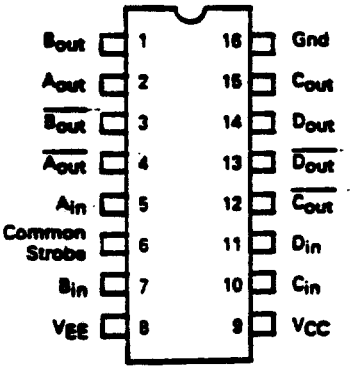
FN SUFFIX
PLCC
CASE 775

LOGIC DIAGRAM



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-31.

3

ELECTRICAL CHARACTERISTICS

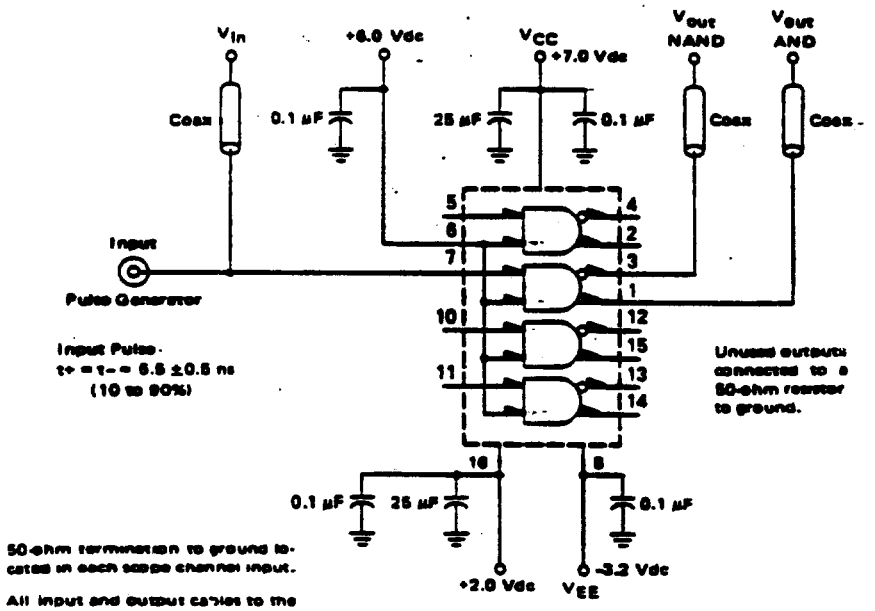
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one translator. The other translators are tested in the same manner.

@ Test Temperature	V_{IH}	$V_{IL\,min}$	V_{IHA}*	V_{ILA}*	V_F	V_R	V_{CC}	V_{EE}	I_I (mA)	I_{in} (mA)
−30°C	+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	−5.2	.10	+1.0
+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	−5.2	.10	+1.0
+85°C	+4.0	+0.40	+1.50	+0.90	+0.40	+2.40	+5.00	−5.2	.10	+1.0

Characteristic	Symbol	Pin Under Test	MC10124 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	V_{IH}	$V_{IL\,max}$	V_{IHA}*	V_{ILA}*	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	8	-	72		-	-66	-	72	mAdc	-	-	-		-	-	9	8	-		16
Positive Power Supply Drain Current	I_{CCH}	9		16		-	16	-	18	mAdc	5,6,7,10,11	-	-		-		9	8			16
	I_{CCL}	9	-	26	-	-	26	-	26	mAdc		-	-		-		9	8			5,6,7,10,11,16
Reverse Current	I_R	6	-	200		-	200	-	200	μAdc	-	-	-		5,7,10,11	6	9	8			16
		7	-	50	-	-	50	-	50	μAdc	-	-			6	7	9	8			16
Forward Current	I_F	6	-	−12.0	-	-	-12.0	-	−12.0	mAdc	5,7,10,11	-	-	-	6		9	8			16
		7	-	−3.2		-	-3.2		-3.2	mAdc	6	-	-		7		9	8			16
Input Breakdown Voltage	BV_{in}	6	5.5		5.5	-	-	5.5	-	Vdc	-	-	-		-		9	8		6	5,7,10,11,16
		7	5.5	-	5.5	-	-	5.5	-	Vdc	-	-			-		9	8		7	6,16
Clamp Input Voltage	V_I	6	-	−1.5	-	-	1.5	-	−1.5	Vdc	-	-	-				9	8	6		16
		7		−1.5		-	1.5		−1.5	Vdc	-	-					9	8	7		16
High Output Voltage	V_{OH}	1	-1.000	-0.890	-0.980	-	-0.810	-0.890	-0.700	Vdc	6,7		-				9	8			16
		3	-1.000	-0.890	-0.980	-	-0.810	-0.890	-0.700	Vdc		6,7					9	8			16
Low Output Voltage	V_{OL}	1	-1.850	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	-	6,7	-				9	8			16
		3	-1.850	-1.675	-1.850	-	-1.650	-1.825	-1.615	Vdc	6,7		-				9	8			16
High Threshold Voltage	V_{OHA}	1	-1.060	-	-0.960	-	-	-0.910	-	Vdc	6		7		-		9	8			16
		3	-1.060	-	-0.960	-	-	-0.910		Vdc	6		-	7			9	8			16
Low Threshold Voltage	V_{OLA}	1	-	-1.655		-	-1.630		-1.595	Vdc	6	-	-	7			9	8			16
		3		-1.655	-	-	-1.630		-1.595	Vdc	6	-	7	-	-		9	8			16
Switching Times (50 Ω load)											+0.8 Vdc	Pulse In	Pulse Out				+7.0 Vdc	3.2 Vdc			+2.0 Vdc
Propagation Delay (1.35 Vdc to 50%)①	t_{p+1+}	1	1.5	6.0	1.0	3.5	6.0	1.0	6.0	ns	7	6	1				9	8			16
	t_{p-1-}		1.0	6.0				1.0	6.0		7	6									
	t_{p+1+}		1.5	6.0				1.0	6.0		6	7									
	t_{p-1-}		1.0	6.0				1.0	6.0												
	t_{p+3+}	3	1.5	6.0				1.0	6.0				3								
	t_{p-3+}	3	1.0	6.0				1.0	6.0												
Rise Time (20% to 80%)	t_{r+}	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3				1								
Fall Time (80% to 20%)	t_f	1			1.1	2.5	3.9						1								

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.)

SWITCHING TIME TEST CIRCUIT



NOTE: All power supply and logic levels are shown shifted 2 volts positive.

3

2

MOTOROLA

MC10125

MECL 10K

QUAD MECL TO TTL TRANSLATOR

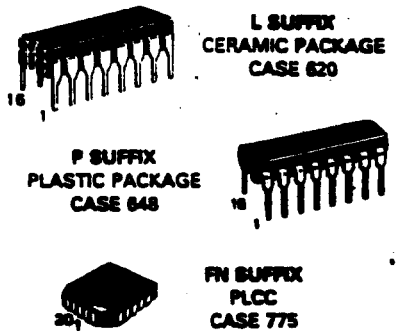
QUAD MECL TO TTL TRANSLATOR

The MC10125 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the MC10125 go to a low logic level whenever the inputs are left floating.

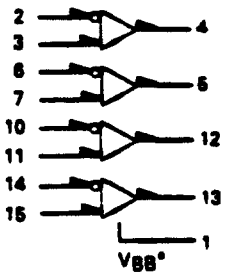
Power supply requirements are ground, +5.0 Volts and −5.2 Volts. Propagation delay of the MC10125 is typically 4.5 ns. The MC10125 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of ± 1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

P_D	= 380 mW typ/pkg (No Load)
t_{pd}	= 4.5 ns typ (50% to + 1.5 Vdc out)
t_r, t_f	= 2.5 ns typ (1.0 V to 2.0 V)



LOGIC DIAGRAM

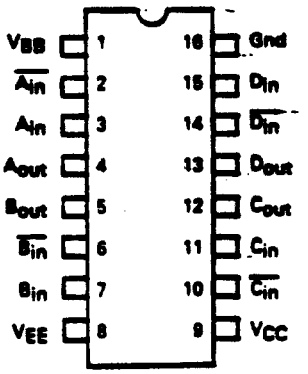


Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (−5.2 Vdc) = Pin 8

*V_{BB} to be used to supply bias to the MC10125 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.

When the input pin with the bubble goes positive the output goes negative.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-31.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one translator. The other translators are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC10125 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Negative Power Supply Drain Current	I_E	8	-	-44	-	-	-40	-	-44	mAdc
Positive Power Supply Drain Current	I_{CCH}	9	-	52	-	-	37	-	52	mAdc
	I_{CCL}	9	-	30	-	-	30	-	30	mAdc
Input Current	I_{inH} ①	2	-	180	-	-	115	-	115	μAdc
Input Leakage Current	I_{CBO}	2	-	1.5	-	-	1.0	-	1.0	μAdc
High Output Voltage	V_{OH}	4	2.5	-	2.5	-	-	2.5	-	Vdc
Low Output Voltage	V_{OL}	4	-	0.5	-	-	0.5	-	0.5	Vdc
High Threshold Voltage	V_{OHA}	4	2.5	-	2.5	-	-	2.5	-	Vdc
Low Threshold Voltage	V_{OLA}	4	-	0.5	-	-	0.5	-	0.5	Vdc
Input Clamp Voltage Protection Tests	V_{OLS1}	4	-	0.5	-	-	0.5	-	0.5	Vdc
	V_{OLS2}	4	-	0.5	-	-	0.5	-	0.5	Vdc
Short-Circuit Current	I_{OS}	4	40	100	40	-	100	40	100	mA
Reference Voltage	V_{BB}	9	-1.420	-1.28	-1.350	-	-1.250	-1.295	-1.160	Vdc
Common Mode Rejection Tests	V_{OH}	4	2.5	-	2.5	-	-	2.5	-	Vdc
		4	2.5	-	2.5	-	-	2.5	-	
	V_{OL}	4	-	0.5	-	-	0.5	-	0.5	Vdc
		4	-	0.5	-	-	0.5	-	0.5	
Switching Times										
Propagation Delay (50% to +1.5 Vdc)	t_{p+0}	6	1.0	6.0	1.0	4.5	6.0	1.0	6.0	ns
	t_{p-0}	6	↓	↓	↓	↓	↓	↓	↓	
	t_{p+4}	4								
	t_{p-4}	4								
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{r+}		-	3.3	-	-	3.3	-	3.3	
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{f-}		-	3.3	-	-	3.3	-	3.3	

① Individually test each input, apply $V_{IH\,max}$ to pin under test

Test Temperature	$V_{IH\,max}$	$V_{IL\,min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.660	+0.110	-0.890	1.890	2.890	From Pin 1	+5.0	-5.2
+25°C	-0.810	-1.850	-1.165	-1.475	+0.190	0.890	1.910	2.890		+5.0	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	+0.300	0.825	1.700	2.825		+5.0	-5.2

TEST VOLTAGE VALUES (Volts)

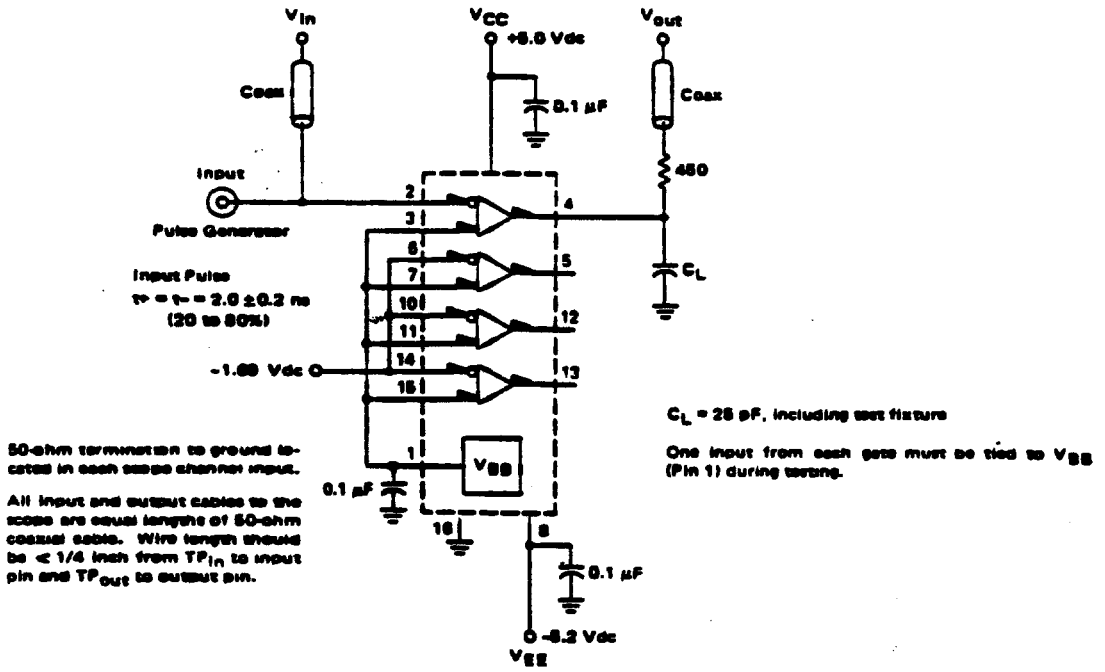
Characteristic	Symbol	$V_{IH\,max}$	$V_{IL\,min}$	V_{IHAmin}	V_{ILAmax}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	-	-	-	-	-	-	-	-	3,7,11,15	9	8	16	-
Positive Power Supply Drain Current	I_{CCH}	2,6,10,14	-	-	-	-	-	-	-	3,7,11,15	9	8	16	-
	I_{CCL}	-	2,6,10,14	-	-	-	-	-	-	3,7,11,15	9	8	16	-
Input Current	I_{inH} ①	2,6,10,14	-	-	-	-	-	-	-	3,7,11,15	9	2,6,8,10,14	16	
Input Leakage Current	I_{CBO}	-	-	-	-	-	-	-	-	3,7,11,15	9	8	16	-20 mA
High Output Voltage	V_{OH}	-	2,6,10,14	-	-	-	-	-	-	3,7,11,15	9	8	16	20 mA
Low Output Voltage	V_{OL}	2,6,10,14	-	-	-	-	-	-	-	3,7,11,15	9	8	16	-20 mA
High Threshold Voltage	V_{OHA}	-	6,10,14	-	2	-	-	-	-	3,7,11,15	9	8	16	20 mA
Low Threshold Voltage	V_{OLA}	6,10,14	-	2	-	-	-	-	-	-	9	2,3,6,7,8,10,11,14,15	16	20 mA
Input Clamp Voltage Protection Tests	V_{OLS1}	-	-	-	-	-	-	-	-	-	9	8	16	20 mA
	V_{OLS2}	-	-	-	-	-	-	-	-	3,7,11,15	9	8	4,16	
Short-Circuit Current	I_{OS}	-	2,6,10,14	-	-	-	-	-	-	3,7,11,15	-	-	-	-
Reference Voltage	V_{BB}	-	2,6,10,14	-	-	-	-	-	-	-	9	8	16	-20 mA
Common Mode Rejection Tests	V_{OH}	-	-	-	-	3	3	-	-	-	9	8	16	-20 mA
		-	-	-	-	-	-	3	3		9	8	16	20 mA
	V_{OL}	-	-	-	-	2	3	-	-		9	8	16	20 mA
		-	-	-	-	-	-	3	3		9	8	16	20 mA
Switching Times		Pulse In	Pulse Out	C_L (pF)										
Propagation Delay (50% to +1.5 Vdc)	t_{p+0}	0	0	25	-	-	-	-	-	3,7,11,15	9	8	16	-
	t_{p-0}	0	0		-	-	-	-	-					-
	t_{p+4}	0	4		-	-	-	-	-					-
	t_{p-4}	4			-	-	-	-	-					-
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{r+}				-	-	-	-	-					-
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{f-}				-	-	-	-	-					-

TEST VOLTAGE APPLIED TO PINS LISTED BELOW

(3)

3

SWITCHING TIME TEST CIRCUIT



MC54/74HC4514

1-of-16 Decoder/Demultiplexer With Address Latch

High-Performance Silicon-Gate CMOS

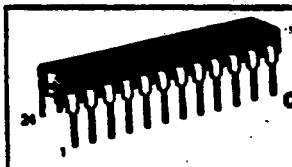
The MC54/74HC4514 is identical in pinout to the MC14514B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of a 4-bit storage latch with a Latch Enable and Chip Select input. When a low signal is applied to the Latch Enable input, the Address is stored, and decoded. When the Chip Select input is high, all sixteen outputs are forced to a low level.

The Chip Select input is provided to facilitate the chip-select, demultiplexing, and cascading functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using the Chip Select as a data input.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 268 FETs or 67 Equivalent Gates



J SUFFIX
CERAMIC
CASE 798-01

N SUFFIX
PLASTIC
CASE 724-03

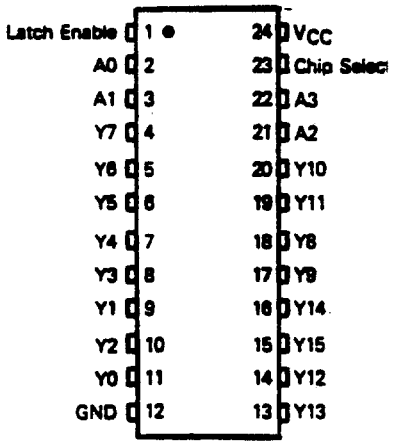
DW SUFFIX
SOIC
CASE 751E-02

ORDERING INFORMATION

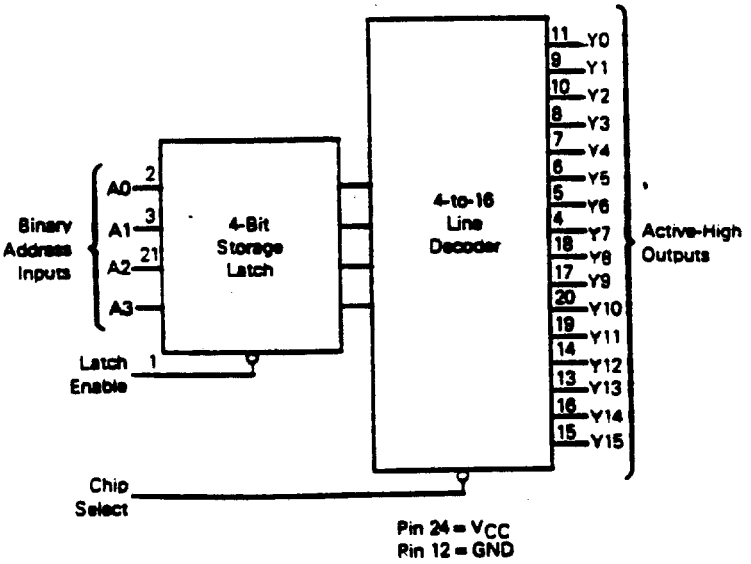
MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

$T_A = -55°$ to $125°C$ for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC}=2.0 V	0	1000	ns
		V_{CC}=4.5 V	0	500	
		V_{CC}=6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions		V_{CC} V	Guaranteed Limit 25°C to −55°C	≤85°C	≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V, $\|I_{out}\|$ ≤ 20 μA		2.0	1.5	1.5	1.5	V
				4.5	3.15	3.15	3.15	
				6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V, $\|I_{out}\|$ ≤ 20 μA		2.0	0.3	0.3	0.3	V
				4.5	0.9	0.9	0.9	
				6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL}, $\|I_{out}\|$ ≤ 20 μA		2.0	1.9	1.9	1.9	V
				4.5	4.4	4.4	4.4	
				6.0	5.9	5.9	5.9	
		V_{in}=V_{IH} or V_{IL}	$\|I_{out}\|$ ≤ 4.0 mA	4.5	3.98	3.84	3.70	
			$\|I_{out}\|$ ≤ 5.2 mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL}, $\|I_{out}\|$ ≤ 20 μA		2.0	0.1	0.1	0.1	V
				4.5	0.1	0.1	0.1	
				6.0	0.1	0.1	0.1	
		V_{in}=V_{IH} or V_{IL}	$\|I_{out}\|$ ≤ 4.0 mA	4.5	0.26	0.33	0.40	
			$\|I_{out}\|$ ≤ 5.2 mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND		6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in}=V_{CC} or GND, I_{out}=0 μA		6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25°C to −55°C	≤85°C	≤125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Chip Select to Output Y (Figures 1 and 5)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 5)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t_{PHL}		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 3 and 5)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t_{PHL}		2.0	175	220	265	
		4.5	35	44	53	
		6.0	30	37	45	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 70	pF

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25°C to −55°C	≤85°C	≤125°C	Unit
t_{su}	Minimum Setup Time, Input A to Latch Enable (Figure 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t_h	Minimum Hold Time, Latch Enable to Input A (Figure 4)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t_w	Minimum Pulse Width, Latch Enable (Figure 3)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

SWITCHING WAVEFORMS

FIGURE 1

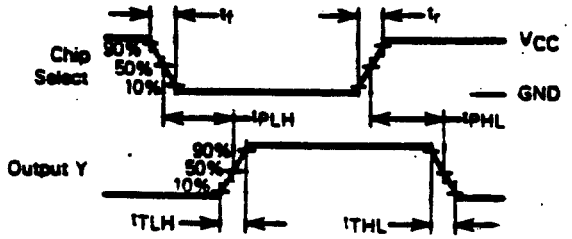


FIGURE 2

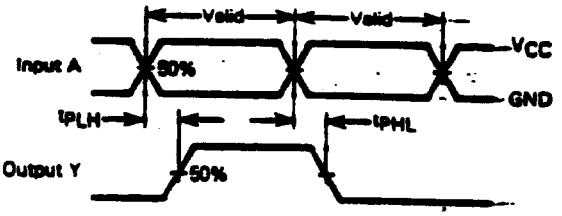


FIGURE 3

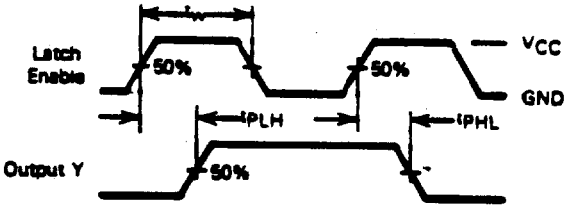


FIGURE 4

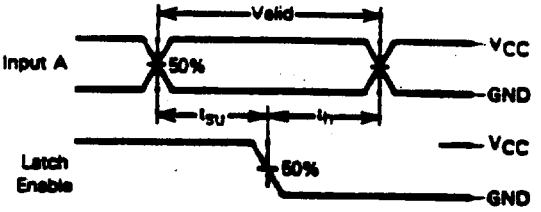
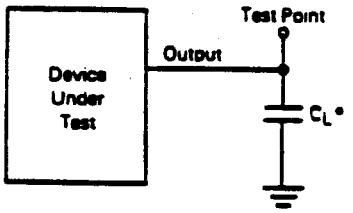


FIGURE 5 — TEST CIRCUIT



* Includes all probe and jig capacitance.

FUNCTION TABLE

Latch Enable	Chip Select	Address Inputs A3	A2	A1	A0	Selected Output (High)
H	L	L	L	L	L	Y0
H	L	L	L	L	H	Y1
H	L	L	L	H	L	Y2
H	L	L	L	H	H	Y3
H	L	L	H	L	L	Y4
H	L	L	H	L	H	Y5
H	L	L	H	H	L	Y6
H	L	L	H	H	H	Y7
H	L	H	L	L	L	Y8
H	L	H	L	L	H	Y9
H	L	H	L	H	L	Y10
H	L	H	L	H	H	Y11
H	L	H	H	L	L	Y12
H	L	H	H	L	H	Y13
H	L	H	H	H	L	Y14
H	L	H	H	H	H	Y15
X	H	X	X	X	X	All Outputs = L
L	L	X	X	X	X	Latched Data

PIN DESCRIPTIONS

ADDRESS INPUTS

A0, A1, A2, A3 (PINS 2, 3, 21, 22) — Address Inputs. These inputs are decoded to produce a high level on one of 16 outputs. The inputs are arranged such that A3 is the most-significant bit and A0 is the least-significant bit. The decimal equivalent of the binary input address indicates which of the 16 data outputs, Y0-Y15, is selected.

OUTPUTS

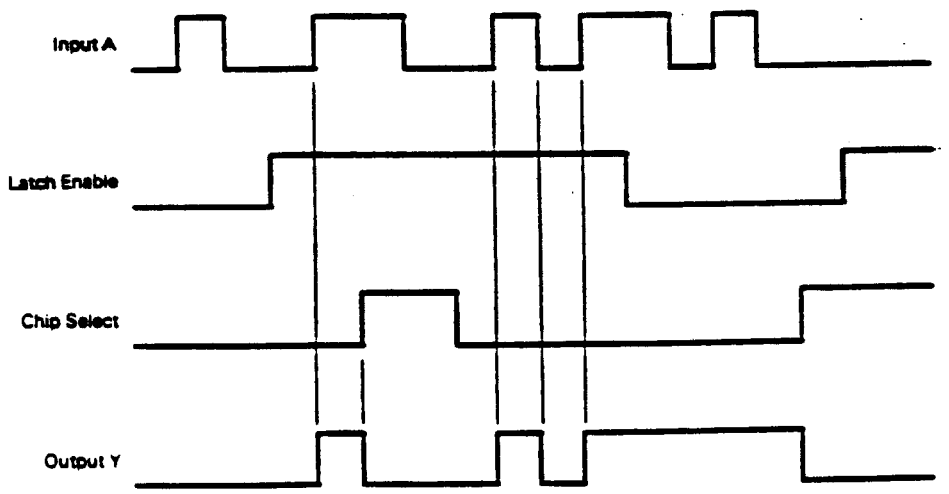
Y0-Y15 (PINS 11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15) — Active-High Outputs. These outputs produce a high level when selected (Latch Enable = H, Chip Select = L) and are at a low level when not selected.

CONTROL INPUTS

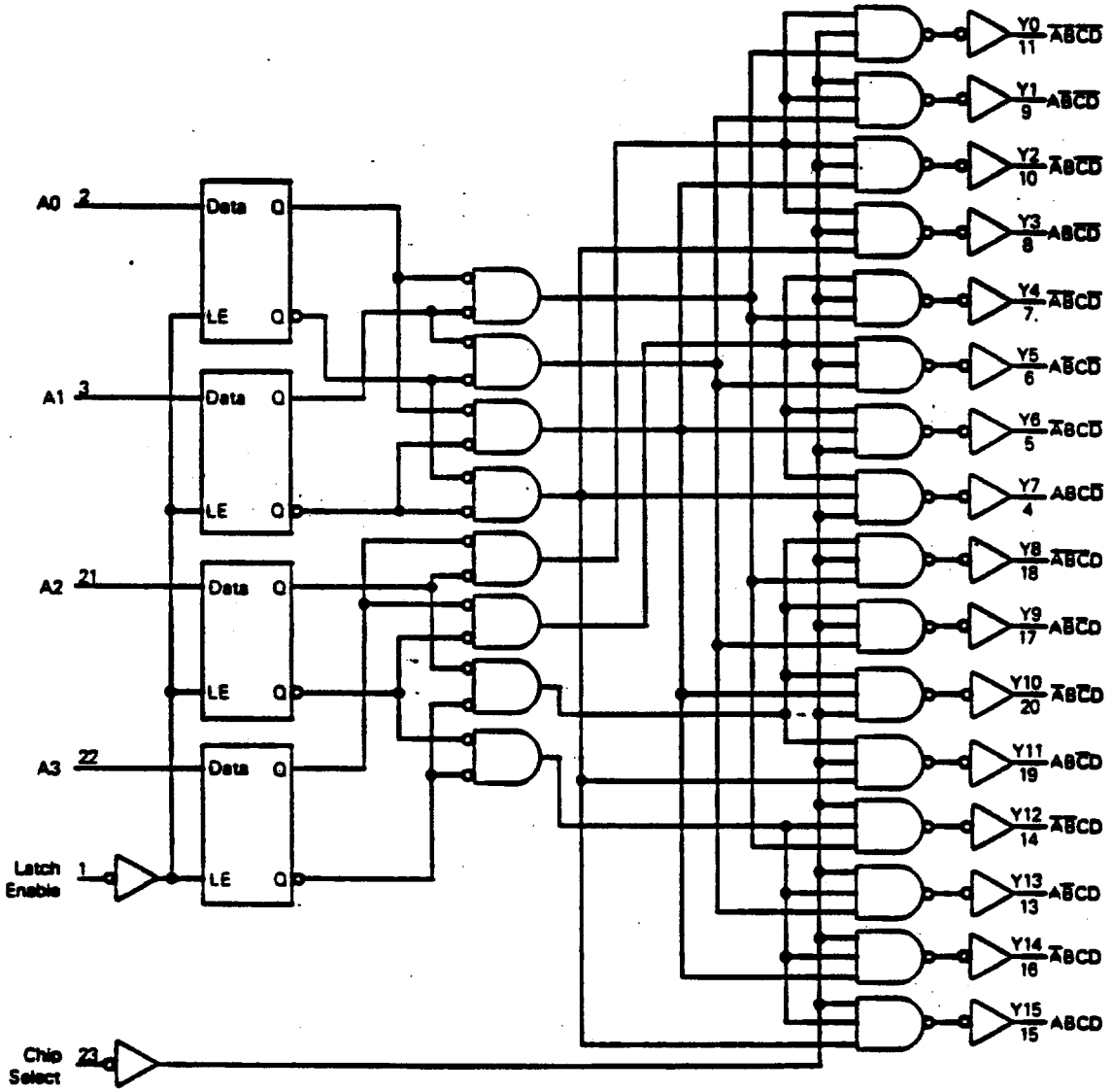
LATCH ENABLE (PIN 1) — Latch Enable Input. A low level on this input stores the data on the Address data inputs in the 4-bit latch. A high level on the Latch Enable input makes the latch transparent and allows the outputs to follow the inputs. Note that the data is latched only while the Latch Enable input is at a low level.

CHIP SELECT (PIN 23) — Chip Select Input. A high on this input produces a low level on all outputs, regardless of what appears at the address or Latch Enable inputs. A low level on the Chip Select input allows the selected output to produce a high level.

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM



MOTOROLA

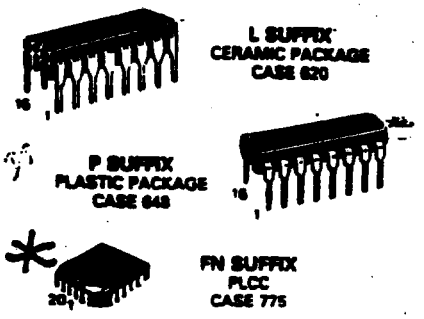
MC10H188

HEX BUFFER WITH ENABLE

The MC10H188 is a high-speed Hex Buffer with a common Enable input. When Enable is in the high-state, all outputs are in the low-state. When Enable is in the low-state, the outputs take the same state as the inputs.

This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical Data-to-Output
- Power Dissipation 180 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0–+75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%) (See Note)

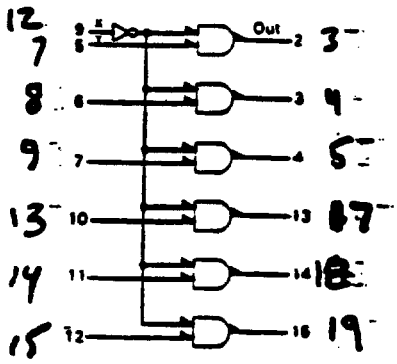
Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	46	—	42	—	46	mA
Input Current High	I_{inH}	—	495	—	310	—	310	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay Enable Data	t_{pd}	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.2 1.9	 0.7 0.7	 2.2 1.9	ns
Rise Time	t_r	0.7	2.4	0.7	2.4	0.7	2.4	ns
Fall Time	t_f	0.7	2.4	0.7	2.4	0.7	2.4	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50 ohm resistor to -2.0 volts.

LOGIC DIAGRAM

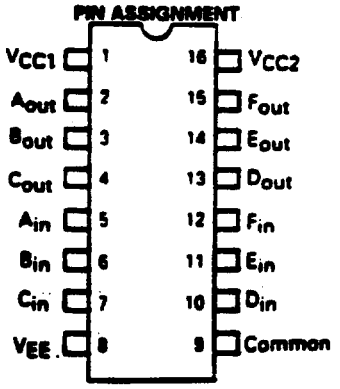


V_{CC1} = Pin 1 2
V_{CC2} = Pin 16 20
V_{EE} = Pin 8 10

TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-31.

10

- **D-C Triggered from Active-High or Active-Low Gated Logic Inputs**
- **Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **'122, 'L122, 'LS122 Have Internal Timing Resistors**

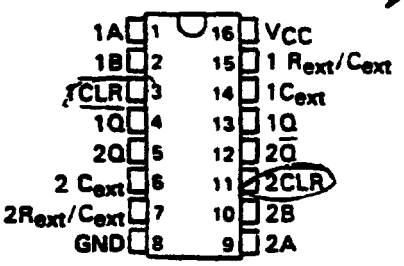
description

These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122, 'L122, and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

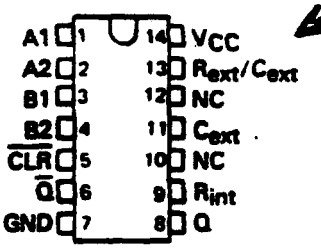
The R_{int} is nominally 10 k ohms for '122, 'LS122, and is nominally 20 k ohms for 'L122.

SN54122, SN54LS122 . . . J OR W PACKAGE
SN54L122 . . . J PACKAGE
SN74122 . . . J OR N PACKAGE
SN74LS122 . . . D, J OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

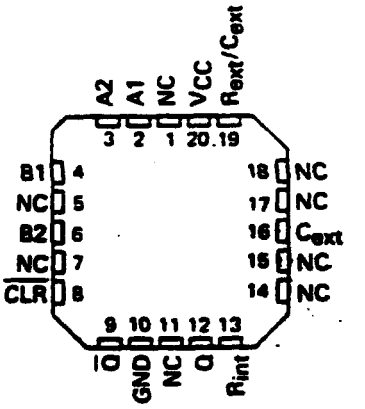


NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of '122, 'L122, or 'LS122, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

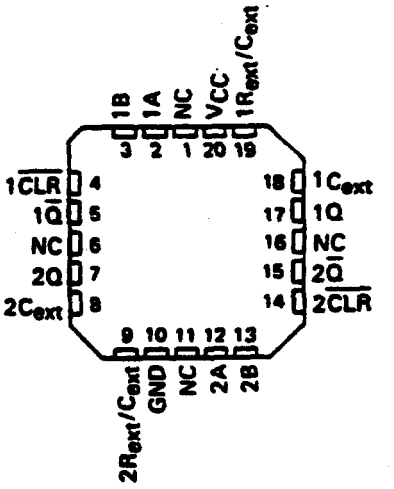
SN54123, SN54130, SN54LS123 . . . J OR W PACKAGE
SN54L123 . . . J PACKAGE
SN74123, SN74130 . . . J OR N PACKAGE
SN74LS123 . . . D, J OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS122 . . . FK PACKAGE
SN74LS122 . . . FN PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS123 . . . FK PACKAGE
SN74LS123 . . . FN PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

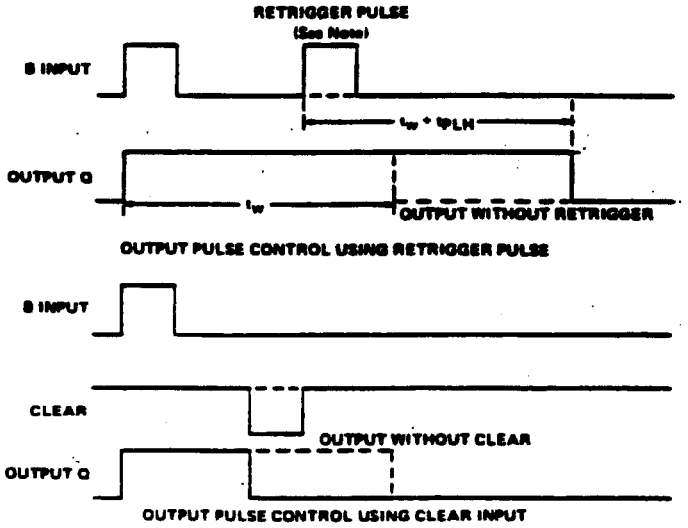


NC - No internal connection

TTL DEVICES

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

escription (continued)



NOTE: Retrigger pulses starting before 0.22 C_{ext} (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output pulse will remain unchanged.

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

'122, 'L122, 'LS122 FUNCTION TABLE

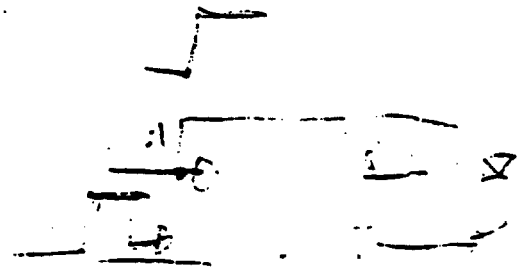
INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

See explanation of function tables on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

'123, '130, 'L123, 'LS123 FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎



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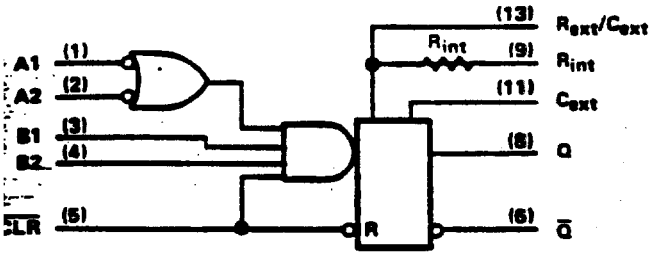
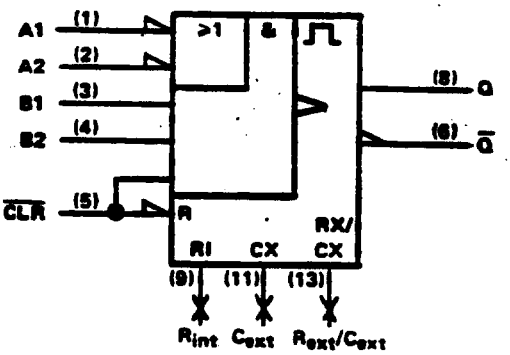
logic diagram

'122, 'L122, 'LS122



logic symbol

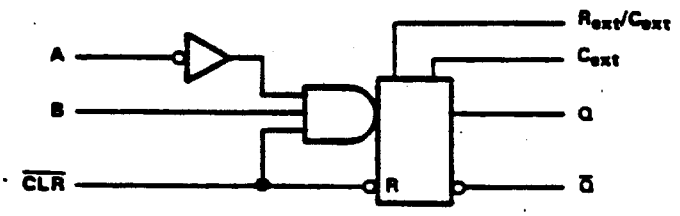
'122, 'L122, 'LS122



R_{int} is nominally 10 k ohms for '122, 'LS122, and 20 k ohms for 'L122.

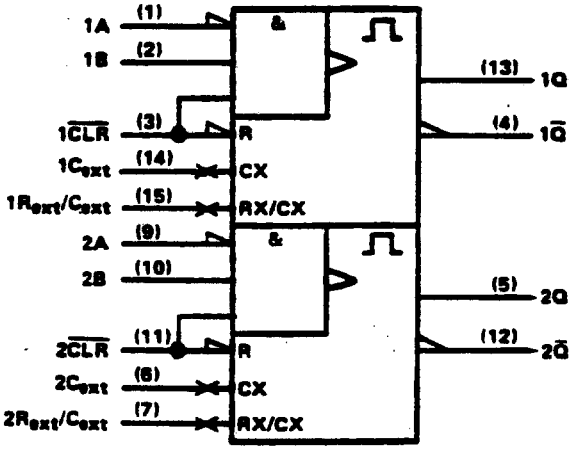
logic diagram (each multivibrator)

'123, '130, 'L123, 'LS123



logic symbol

'123, '130, 'L123, 'LS123



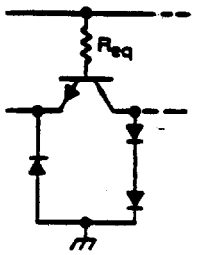
Pin numbers shown on logic notation are for D, J or N packages.

TTL DEVICES

schematics of inputs and outputs

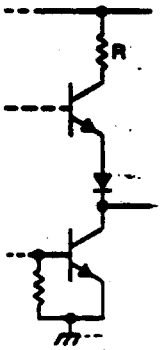
'122, '123, '130, 'L122, 'L123 CIRCUITS

EQUIVALENT OF EACH INPUT



Clear inputs of '122, '123, '130: R_{eq} = 2 kΩ NOM
Other inputs of '122, '123, '130: R_{eq} = 4 kΩ NOM
Clear inputs of 'L122, 'L123: R_{eq} = 4 kΩ NOM
Other inputs of 'L122, 'L123: R_{eq} = 8 kΩ NOM

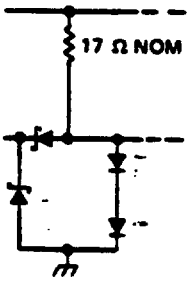
TYPICAL OF ALL OUTPUTS



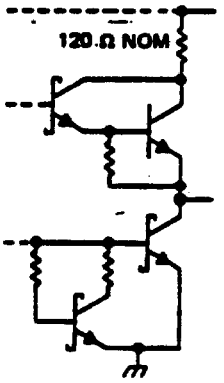
'122, '123, '130: R = 100 Ω NOM
'L122, 'L123: R = 200 Ω NOM

'LS122, 'LS123 CIRCUITS

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



3 TTL DEVICES

TEXAS INSTRUMENTS
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(11)

recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		25	5		50	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'122			'123, '130			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA, See Note 1	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA, See Note 1		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Data inputs	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Clear input				80			80	
I_{IL}	Low-level input current	Data inputs	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Clear input				−3.2			−3.2	
I_{OS}	Short-circuit output current¶		V_{CC} = MAX, See Note 5	−10		−40	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7		23	36		46	66	mA

†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 is open.
7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 8

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'122, '130			'123			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF, R_{ext} = 5 kΩ, R_L = 400 Ω		22	33		22	33	ns
	B				19	28		19	28	
t_{PHL}	A	$\overline{Q}$			30	40		30	40	ns
	B				27	36		27	36	
t_{PHL}	Clear	Q			18	27		18	27	ns
t_{PLH}		$\overline{Q}$			30	40		30	40	
t_{wQ} (min)	A or B	Q			45	65		45	65	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF, R_{ext} = 10 kΩ, R_L = 400 Ω	3.08	3.42	3.76	2.76	3.03	3.37	μs

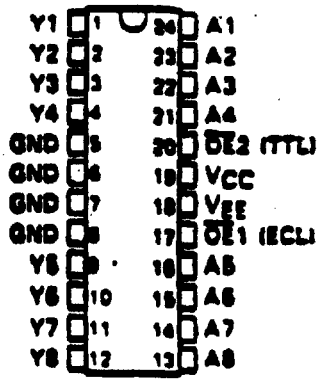
¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q

NOTE 8: See General Information Section for load circuits and voltage waveforms.

TTL DEVICES

- 10KH Compatible
- ECL and TTL Control Inputs
- P-N-P Inputs Reduce DC Loading
- New Flow-Through Architecture to Optimize PCB Layout
- Center Pin V_{CC}, V_{EE} and GND Configurations to Minimize High-Speed Switching Noise
- ESD Protection Exceeds 2000 V, MIL-STD-883C Method 3015
- Package Options Include "Small Outline" Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

These octal TTL-to-ECL translators are designed to provide an efficient translation function between a TTL signal environment and a 10KH ECL signal environment. The designer has a choice of inverting ('5542) or true ('5543) outputs. Two pins, $\overline{OE1}$ and $\overline{OE2}$, are provided for output enable control. These control inputs are negative ANDed together, with $\overline{OE1}$ being ECL compatible and $\overline{OE2}$ being TTL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment. The outputs, when disabled, go to a normal ECL logic low level.

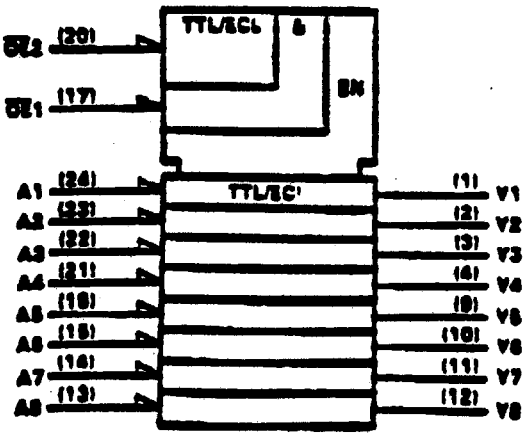
The SN10KHT5542 and SN10KHT5543 are characterized for operation from 0°C to 75°C.

FUNCTION TABLE

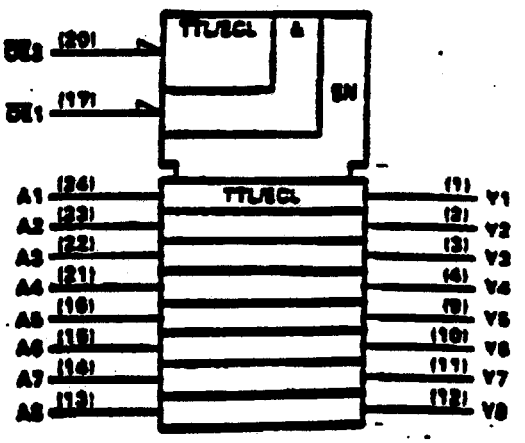
OUTPUT CONTROL		DATA INPUT	OUTPUT	
$\overline{OE1}$	$\overline{OE2}$	A	'5542	'5543
H	X	X	L	L
X	H	X	L	L
L	L	L	H	L
L	L	H	L	H

logic symbols†

SN10KHT5542



SN10KHT5543



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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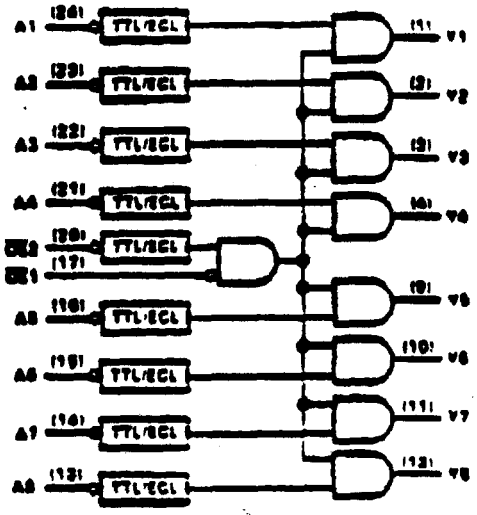
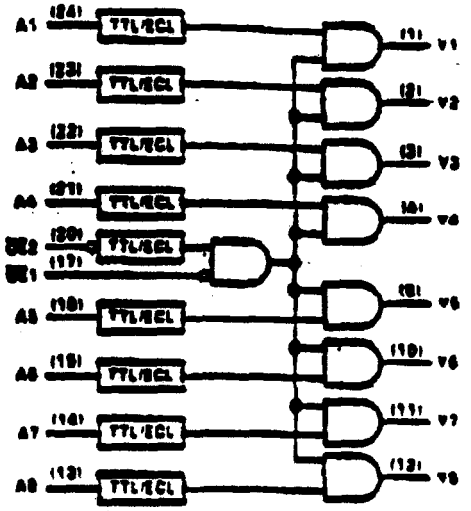
logic diagrams (positive logic)

SN10KHT5542



SN10KHT5543



absolute maximum ratings over operating ambient temperature range (unless otherwise noted

Supply voltage, V_{CC}	−0.5 V to
Supply voltage, V_{EE}	−8 V to
Input voltage (TTL) (See Note 1)	−1.2 V to
Input voltage (ECL)	V_{EE} to
Input current (TTL)	−30 mA to 5
Operating ambient temperature range	0°C
Storage temperature range	−65°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ra only and functional operation of the device at these or any other conditions beyond those indicated under "recommended oper conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	U
V_{CC}	TTL supply voltage		4.5	5.0	5.5	V
V_{EE}	ECL supply voltage		−4.94	−5.2	−5.46	V
V_{IH}	TTL high-level input voltage		2			V
V_{IH}	ECL high-level input voltage‡	0°C	−1170		−840	m
		25°C	−1130		−810	
		75°C	−1070		−735	
V_{IL}	TTL low-level input voltage				0.8	V
V_{IL}	ECL low-level input voltage‡	0°C	−1950		−1480	m
		25°C	−1950		−1480	
		75°C	−1950		−1450	
I_{IK}	TTL input clamp current				−18	m
T_A	Operating ambient temperature (see Note 3)		0		75	°C

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for voltage levels and temperature only.

NOTES: 2. If unused, OE1 should be tied directly to −2 V.
3: Each 10KH series circuit has been designed to meet the dc specifications shown in the electrical characteristics table thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board, and transv air flow greater than 500 linear ft/min is maintained.

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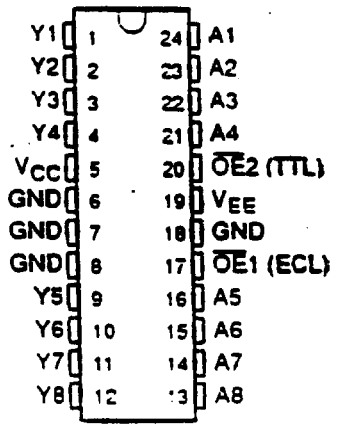
DXXXX, JULY 1989 COMPOSED JUL 20, 1989 AT 10:32:14

- 10KH Compatible
- ECL and TTL Control Inputs
- New Flow-Through Architecture to Optimize PCB Layout
- Center Pin V_{CC}, V_{EE} and GND Configurations to Minimize High Speed Switching Noise
- ESD Protection Exceeds 2000 V, Mil Standard 883C Method 3015
- Package Options Include "Small Outline" Packages, Standard Plastic and Ceramic 300-mil DIPs

SN10KHT5540...DW or NT Package
SN10KHT5541...DW or NT Package
(TOP VIEW)



description

These octal ECL-to-TTL translators are designed to provide the efficient translation function between a 10KH ECL signal environment to a TTL signal environment. These devices are designed specifically to improve the performance and density of ECL-to-TTL CPU/Bus oriented functions such as memory address drivers, clock drivers, and bus oriented receivers and transmitters.

The designer has a choice of inverting ('5540) or true ('5541) outputs. Two pins $\overline{OE}1$ and $\overline{OE}2$ are allowed for output enable control. These control inputs are or'ed together with $\overline{OE}1$ being TTL compatible and $\overline{OE}2$ being ECL compatible. This offers the choice of controlling the outputs of the device from either a TTL or ECL signal environment.

The SN10KHT5540 and SN10KHT5541 are characterized for operation from 0°C to 75°C.

PRELIMINARY

FUNCTION TABLE

OUTPUT CONTROL		DATA INPUT	OUTPUT	
$\overline{OE}1$	$\overline{OE}2$	A	'5540	'5541
X	H	X	Z	Z
H	X	X	Z	Z
L	L	L	H	L
L	L	H	L	H

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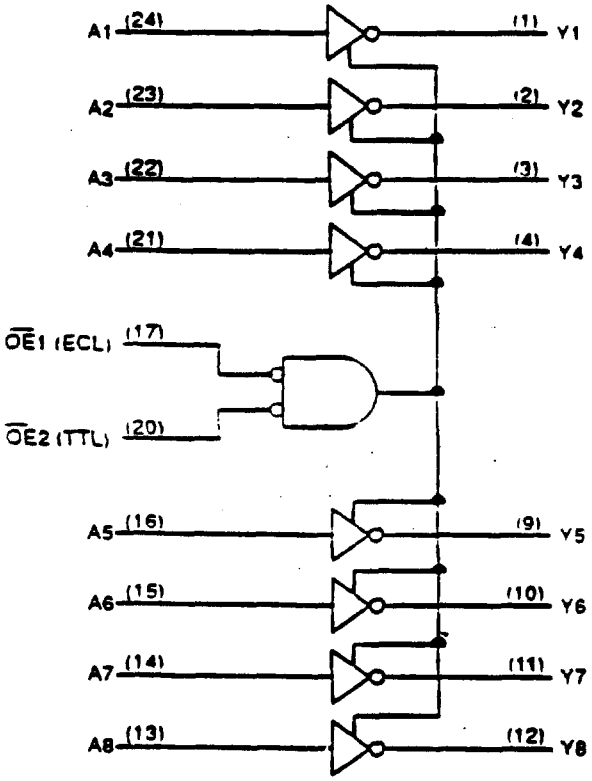
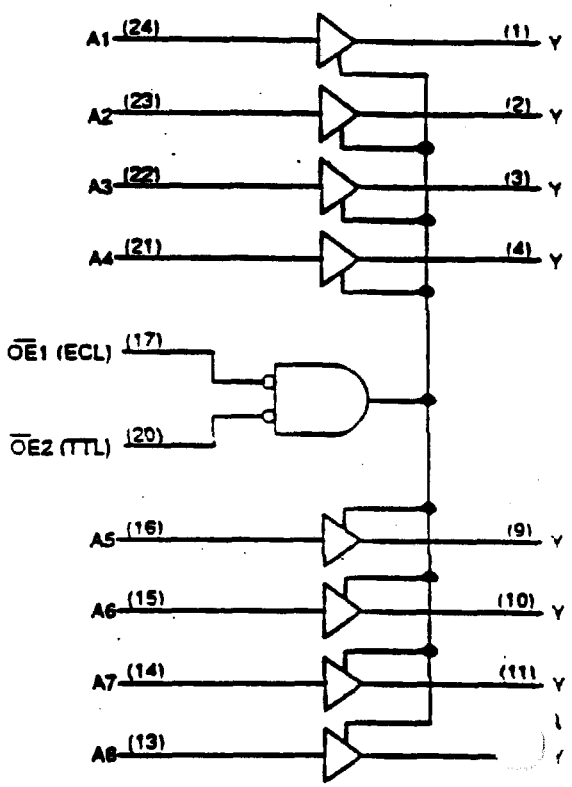
logic diagram (positive logic)

SN10KHT5540



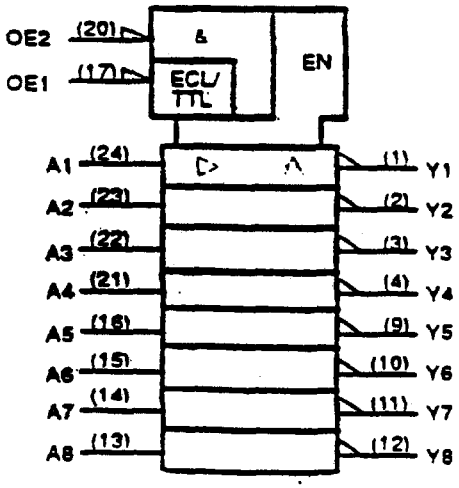
SN10KHT5541



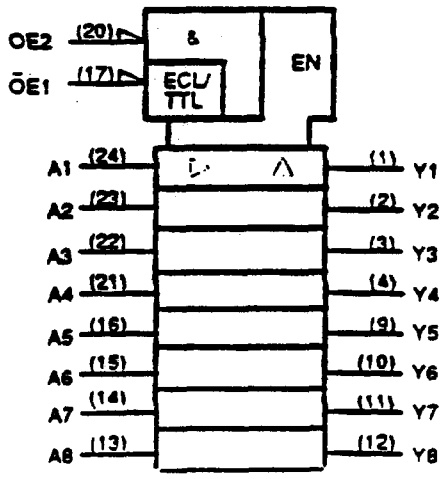
logic symbols*

PRELIMINARY

SN10KHT5540



SN10KHT5541



*These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EPM5016 to EPM5192

High-Speed, High-Density MAX EPLDs

October 1990, ver. 1 — Data Sheet

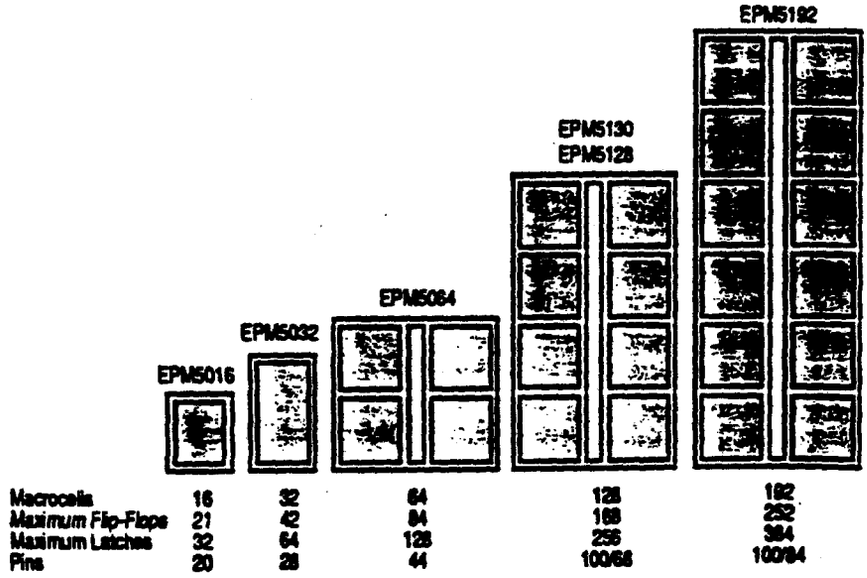
Features

- Complete family of CMOS EPLDs solves design tasks ranging from fast 20-pin address decoders to 100-pin LSI custom peripherals.
- The advanced MAX architecture combines the speed, ease of use, and familiarity of PAL devices with the density of programmable gate arrays.
- EP5000-series EPLDs provide 15-ns combinatorial delays, counter frequencies up to 100 MHz, pipelined data rates of 100 MHz, and high-complexity designs with true system clock rates up to 66 MHz.
- Available in a wide variety of packages, including DIP, SOIC, J-Lead, PGA, and QFP formats in windowed ceramic and plastic one-time-programmable versions.
- MAX+PLUS PC- and workstation-based development tools compile large designs in minutes.
- Industry-standard EDIF interfaces to workstation and third-party CAE tools are available.

3

Figure 1 shows the EPM5000-series modular architecture.

Figure 1. EPM5000-Series Modular Architecture



14

Family Highlights

- **Multiple Array MatriX (MAX) architecture solves speed, density, and design flexibility problems**
  - Advanced macrocell array provides registered, combinatorial, or flow-through latch operation.
  - Expander product-term array automatically provides additional combinatorial or registered logic.
  - Decoupled I/O block with dual feedback on I/O pins allows flexible pin utilization.
  - Programmable Interconnect Array provides automatic 100% routing in devices with multiple LABs.
  - Each macrocell supports synchronous or asynchronous operation of every macrocell, using single or multiple clocks per device.
- EPM5000-Series Performance
  - Pipelined data rates up to 100 MHz
  - Counters as fast as 100 MHz
  - t_{PD} performance from 15 ns to 25 ns
  - Advanced 0.8-micron CMOS EPROM technology
- EPM5000-Series Logic Density
  - 16- to 192-macrocell devices
  - 20- to 100-pin packages
  - 32 to 384 flip-flops and latches
  - More than 32 product terms on a single macrocell
  - Product-term expansion on any data or control path
- MAX+PLUS Design Tools
  - Design entry via unified, hierarchical schematic capture and Altera Hardware Description Language (AHDL)
  - Fast, automatic design processing with logic synthesis
  - Automatic device fitting, no hand editing needed
  - Hardware and software design verification tools
  - Compiles a 16-bit counter in 34 seconds on a 16-MHz 386 computer
- EDIF interfaces to MAX+PLUS provide paths to Dazix, Valid Logic Systems, Mentor Graphics, and other workstation-based CAE tools.

General Description

EPM5000-series Erasable Programmable Logic Devices (EPLDs) represent a revolutionary step in programmable logic: they combine innovative architecture and state-of-the-art process to offer optimum performance, logic density, flexibility, and the highest speeds and densities available in general-purpose reprogrammable logic. These EPLDs are high-speed, high-density replacements for SSI and MSI TTL and CMOS packages and conventional PLDs. For example, an EPM5192 replaces over 100 7400-series SSI and MSI TTL and CMOS packages, integrating complete subsystems into a single package, saving board area, and reducing power consumption.

These MAX EPLDs range in density from 16 to 192 macrocells. They are divided into two groups: higher-speed MAX EPLDs (EPM5016 and EPM5032) and higher-density MAX EPLDs (EPM5064, EPM5128, EPM5130 and EPM5192). The higher-speed MAX EPLDs achieve system c[illegible] frequencies of 66 MHz, and are capable of counter frequencies of 100 M[illegible]

Logic Array Blocks The EPM5016 and EPM5032 MAX EPLDs have a single Logic Array Block (LAB). The EPM5064, EPM5128, EPM5130, and EPM5192 MAX EPLDs contain multiple LABs. Each LAB contains a macrocell array, an expander product-term array, and a decoupled I/O block. Expander product terms (expanders) are unallocated, inverted product terms that can be used and shared by all macrocells in the LAB to create combinatorial and registered logic. Thus, expressions requiring up to 66 product terms can be implemented in a single macrocell. Signals in the higher-density devices are routed between multiple LABs by a Programmable Interconnect Array (PIA) that ensures 100% routability. This multiple array architecture enables EPM5000-series EPLDs to offer the speed of smaller arrays with the integration density of larger arrays.

Modular Architecture The modular architecture of MAX EPLDs provides integration solutions over a wide range of logic densities. Migration from one type of device to another is easy. For example, the EPM5128 and EPM5130 EPLDs have the same logic capacity, but have packages optimized to handle different I/O requirements. Over the entire family, a wide range of packaging options for both through-hole and surface-mount applications is available. Plastic one-time-programmable (OTP) packages are available for economical volume production.

3

Logic Design Entry Logic designs are created and programmed into EPM5000-series EPLDs with the MAX+PLUS Development System. MAX+PLUS is a complete CAE system offering hierarchical design entry tools, automatic design compilation and fitting, timing simulation, and device programming. The MAX+PLUS Compiler features advanced logic synthesis algorithms, allowing designs to be entered in a variety of high-level formats while ensuring the most efficient use of EPLD resources. The combination of a flexible architecture and advanced CAE tools ensures rapid design cycles so that a design may go from conception to completion in single day. Interfaces to third-party tools are also available to allow design entry and logic simulation on a variety of workstation platforms.

Functional Description

EPM5000-series EPLDs use CMOS EPROM cells to configure logic functions within the devices. MAX architecture is user-configurable to accommodate a variety of independent logic functions, and the EPLDs can be erased for quick and efficient iterations during design development and debug cycles.

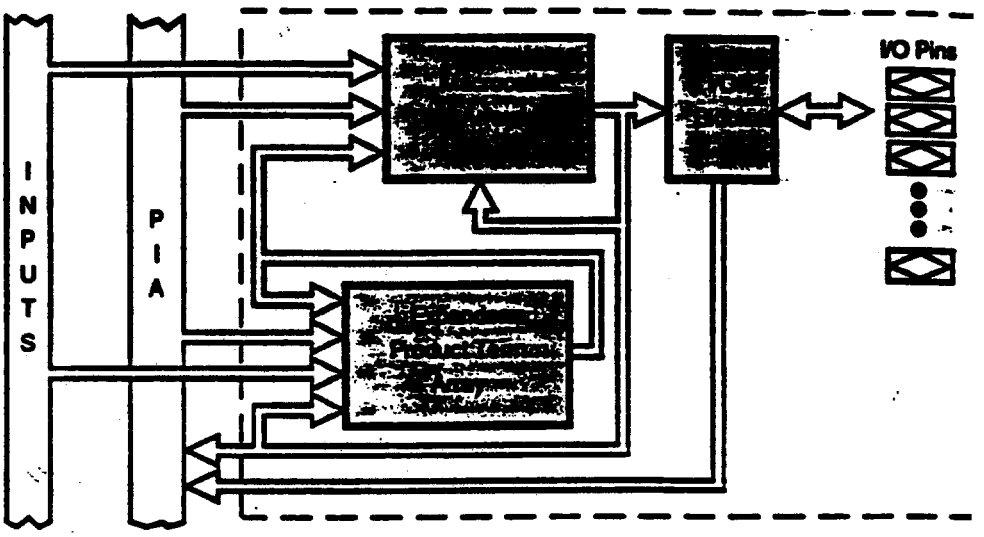
Logic Array Block

EPM5000-series EPLDs contain from 1 to 12 Logic Array Blocks. Each LAB, shown in Figure 2, consists of a macrocell array, an expander product-term array, and an I/O control block. (The number of macrocells and expanders in the arrays varies with each device.) Macrocells are the primary resource for logic implementation, but if needed, expanders can be used to supplement the capabilities of any macrocell. The expander product-term array consists of a group of unallocated, inverted product terms. Flexible macrocells and allocatable expanders facilitate variable product-term designs

(14

Figure 2. Logic Array Block

The LAB consists of a macrocell array, an expander product-term array, and a decoupled I/O block. The flexibility of the LAB ensures high speeds and efficient device utilization.



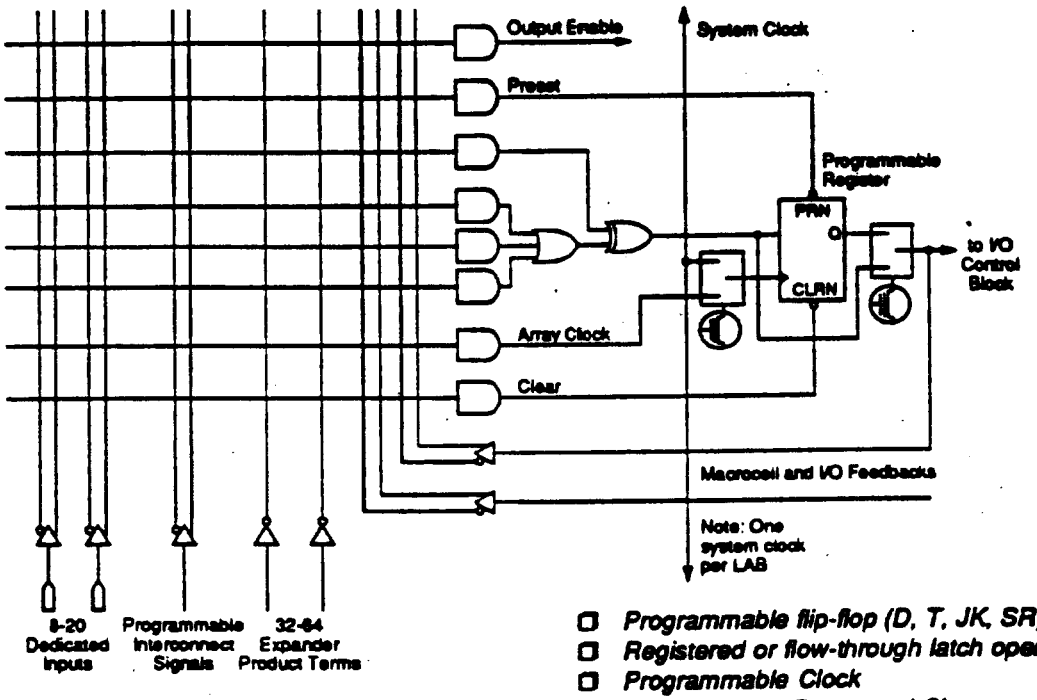
without the waste associated with fixed product-term architectures. Thus PAL or PLA devices are easily integrated into MAX EPLDs. The outpu o the macrocells feed the decoupled I/O block, which consists of a gr programmable tri-state buffers and I/O pins. In the EPM5064, EP EPM5130, and EPM5192, multiple LABs are connected by a Programmabl Interconnect Array (PIA).

Macrocells

The EPM5000-series macrocell, shown in Figure 3, consists of programmable logic array and an independently configurable register. Thi register may be programmed for D, T, JK, or SR operation; or as a flow through latch; or bypassed for purely combinatorial operation Combinatorial logic is implemented in the programmable logic array, whic consists of three product terms ORed together that feed one input of an XO gate. The second input to the XOR gate is also controlled by a product term that makes it possible to implement active-high or active-low logic. The XO gate is also used for complex XOR arithmetic logic functions and fo De Morgan's inversion to reduce the number of product terms. The outpu of the XOR gate feeds the programmable register, or bypasses it for purel combinatorial operation. The logic array ensures high speed whil eliminating inefficient, unused product terms. Also, expanders can b allocated to enhance the capability of the logic array.

Additional product terms, called secondary product terms, are used fo Output Enable, Preset, Clear, and Clock logic. Preset and Clear produc terms drive the active-low asynchronous Preset and asynchronous Clea inputs to the configurable flip-flop. The Clock product term allo register to have an independent Clock and supports positive- and

Figure 3. EPM5000-Series Macrocell



- *Programmable flip-flop (D, T, JK, SR)*
- *Registered or flow-through latch operation*
- *Programmable Clock*
- *Asynchronous Preset and Clear*

edge-triggered operation. Macrocells that drive an output pin may use the Output Enable product term to control the active-high tri-state buffer in the I/O control block. These secondary product terms allow 7400-series TTL functions to be emulated exactly.

The EPM5000-series macrocell configurability makes it possible to efficiently integrate complete subsystems into a single device. All macrocell outputs are globally routed within an LAB and also feed the PIA to provide efficient routing of signal-intensive designs.

Clock Options

Each LAB has two clocking modes: asynchronous and synchronous. During asynchronous clocking, each flip-flop is clocked by a product term. Thus, any input or internal logic may be used as a clock. Systems that require multiple clocks are easily integrated into EPM5000-series EPLDs. Asynchronous clocking also allows each flip-flop to be configured for positive- or negative-edge-triggered operation, giving the macrocell a high degree of flexibility.

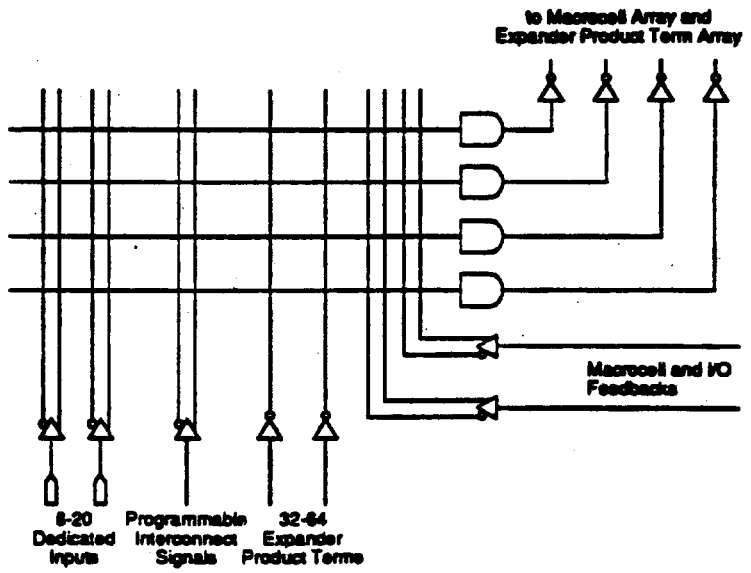
Synchronous clocking is provided by a dedicated system clock (**CLK**). This direct connection provides enhanced clock-to-output delay times. Since each LAB has one synchronous clock, all flip-flop clocks within it are positive-edge-triggered from the **CLK** pin. If the **CLK** pin is not used as a system clock, it may be used as a dedicated input.

Expander Product Terms

The expander product-term array (Figure 4) contains unallocated, invertec product terms that enhance the macrocell array. Expanders can be used anc shared by all product terms in the LAB. Wherever extra logic is neede (including register control functions), expanders can be used to implemen the logic. These expanders provide the flexibility to implement register intensive and product-term-intensive designs for MAX EPLDs.

Figure 4. Expander Product Terms

Expander product terms are unallocated logic that can be used and shared by all macrocells in an LAB. Sharing allows efficient integration of complex combinatorial functions.



Expanders are fed by all signals in the LAB. One expander may feed al macrocells in the LAB or multiple product terms in the same macrocell Since expanders also feed the secondary product terms of each macrocell complex logic functions can be implemented without using anothe macrocell. Expanders can be cross-coupled to build additional flip-flops o latches.

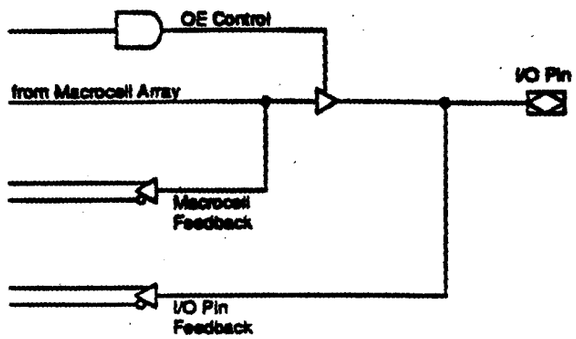
I/O Control Block

Each LAB has an I/O control block (Figure 5) that consists of a user-configurable I/O control function for each I/O pin. The I/O control block i fed by the macrocell array. The tri-state buffer is controlled by a dedicatec macrocell product term, and drives the I/O pad.

Each MAX EPLD has dual feedback—one feedback path before and on after the tri-state buffer— for every I/O pin. The tri-state buffer decouple the I/O pins from the macrocells so that all registers within the LAB can b "buried." Thus, I/O pins can be configured as dedicated input, output, or bidirectional pins. In multiple-LAB MAX devices, I/O pins feed the PIA.

Figure 5. I/O Control Block

The decoupled I/O control block features dual feedback to maximize use of device pins.



Programmable Interconnect Array

The higher-density EPM5000-series devices (EPM5064, EPM5128, EPM5130, and EPM5192) use a Programmable Interconnect Array (PIA) to route signals between the various LABs. The PIA routes only the signals required for implementing logic in an LAB, and is fed by all macrocell feedbacks and all I/O pin feedbacks. Unlike channel routing in masked or programmable gate arrays—where routing delays are variable and path-dependent—the PIA has a fixed delay. Because the PIA eliminates skew between signals, timing performance is easy to predict.

3

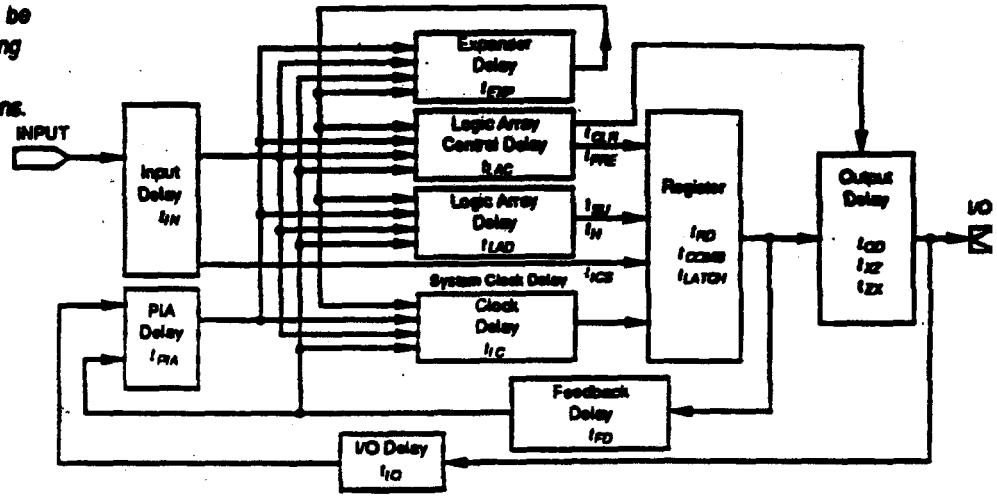
Timing Model

Timing within EPM5000-series EPLDs is easily determined with MAX+PLUS software or with the models shown in Figure 6. EPM5000-series EPLDs have fixed internal delays, that allow the user to determine the worst-case timing delays for any design. For complete timing information, MAX+PLUS software provides a timing simulator, a delay predictor, and a detailed timing analyzer.

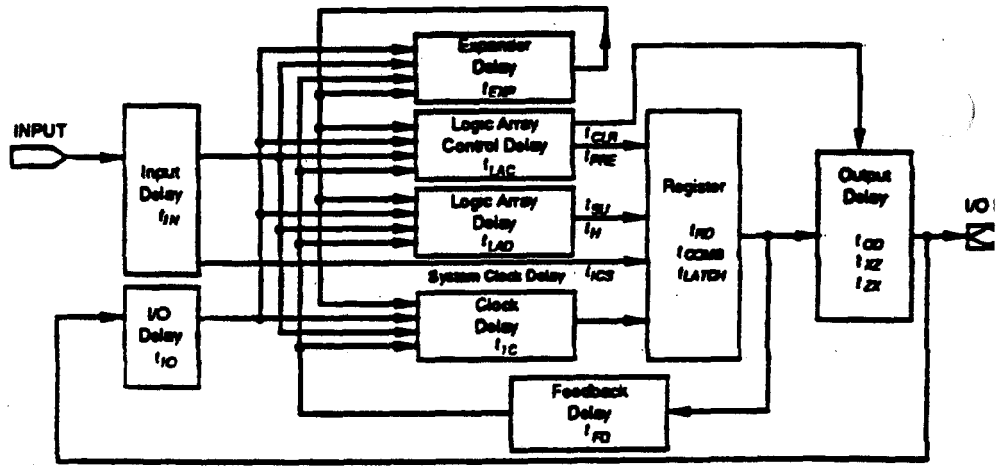
Figure 6. Timing Models

Design performance can be predicted with these timing models and the device performance specifications.

Multiple-LAB EPLDs



Single-LAB EPLDs



The timing models shown in Figure 6 may be used together with the interna timing parameters for a particular EPLD to derive timing informatior External timing parameters are derived from a sum of internal parameter and represent pin-to-pin timing delays. Figure 7 shows the internal timin waveforms for these devices. Refer to *Application Brief 75 (EPM5000-Serie MAX EPLD Timing)* in this data book for further information.

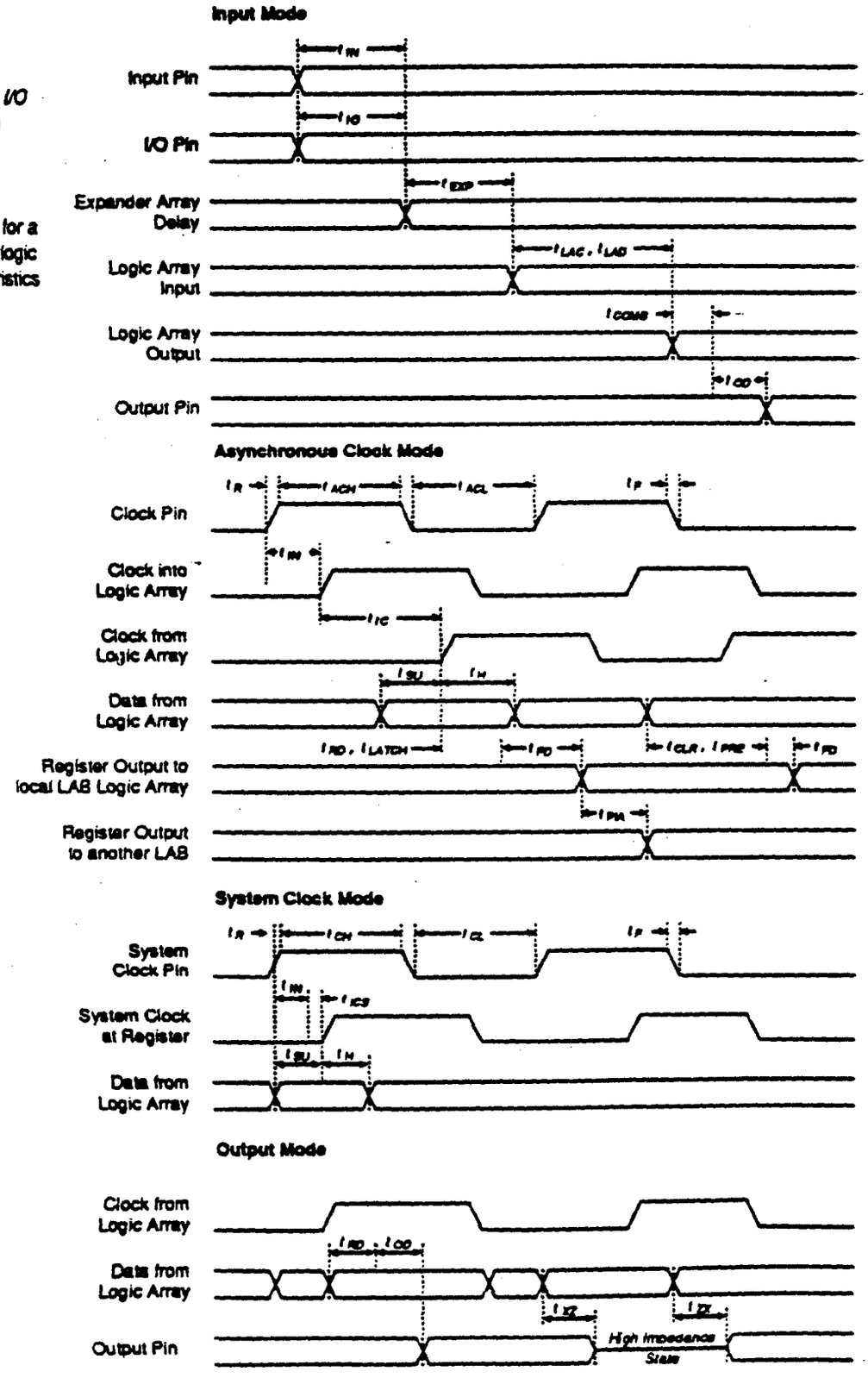
Design Security

MAX EPLDs contain a programmable Security Bit that controls access to th data programmed into the device. If this feature is used, a proprietar design implemented in the device cannot be copied or retrieved. Thi feature provides a high level of design security, since programme within EPROM cells is invisible. The Security Bit that controls this fur as well as all other program data, is reset by erasing the EPLD.

Figure 7. Switching Waveforms

In multiple LAB EPLDs, I/O pins used as inputs can traverse the PIA.

t_R & t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



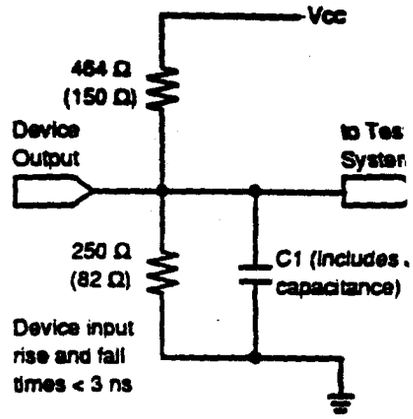
3

MAX EPLDs are fully functionally tested and guaranteed. Complete tes of each programmable EPROM bit and all internal logic elements ensu 100% programming yield. AC test measurements are performed under conditions shown in Figure 8.

Figure 8. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests should not be performed under AC conditions. Large-amplitude, fast-ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable input noise immunity.

Note: Numbers in parentheses are for the EPM5016.



Test programs may be used and then erased during early stages of th production flow. This facility to use application-independent, gen purpose tests is called generic testing and is unique among user-config logic devices. EPLDs also contain on-board logic test circuitry to allov verification of function and AC specifications once they are packaged i windowless packages.

MAX+PLUS Development System

The MAX+PLUS Development System is a unified CAE system fo integrating designs into EPM5000-series MAX EPLDs. Designs can be entered as logic schematics with the Graphic Editor or as state machines, truth tables, and Boolean equations with the Altera Hardware Description Language (AHDL). Logic synthesis and minimization optimize the logic of a design. Design verification and timing analysis are performed with the Simulator or the delay prediction feature. Errors in a design are automatically located and highlighted in the schematic or text design file. Hosted on IBM PS/2, PC-AT, or compatible machines, and workstations (e.g., Apollo, Sun, IBM), MAX+PLUS gives the designer the tools to quickly and efficiently create complex logic designs. Further details about the MAX+PLUS Development System are available in the *PLS-MAX Data Sheet*.

Device Programming

EPM5000-series EPLDs may be programmed on an IBM PS/2, PC-AT or compatible computer with an Altera Logic Programmer card, the PLE3-12A Master Programming Unit, and an appropriate device adapter. These are included in the complete PLDS-MAX Development System o purchased separately. EPM5000-series EPLDs may also be p with third-party hardware (see the *Third-Party Developme Support Data Sheet* in this data book). Contact Altera equipment manufacturer for more information.

Features

- High-density 128-macrocell general-purpose MAX EPLD
- 256 shareable expander product terms that allow over 32 product terms in a single macrocell
- High-speed multiple-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- Available in 68-pin windowed ceramic or plastic one-time-programmable J-lead packages and in 68-pin windowed ceramic PGA packages

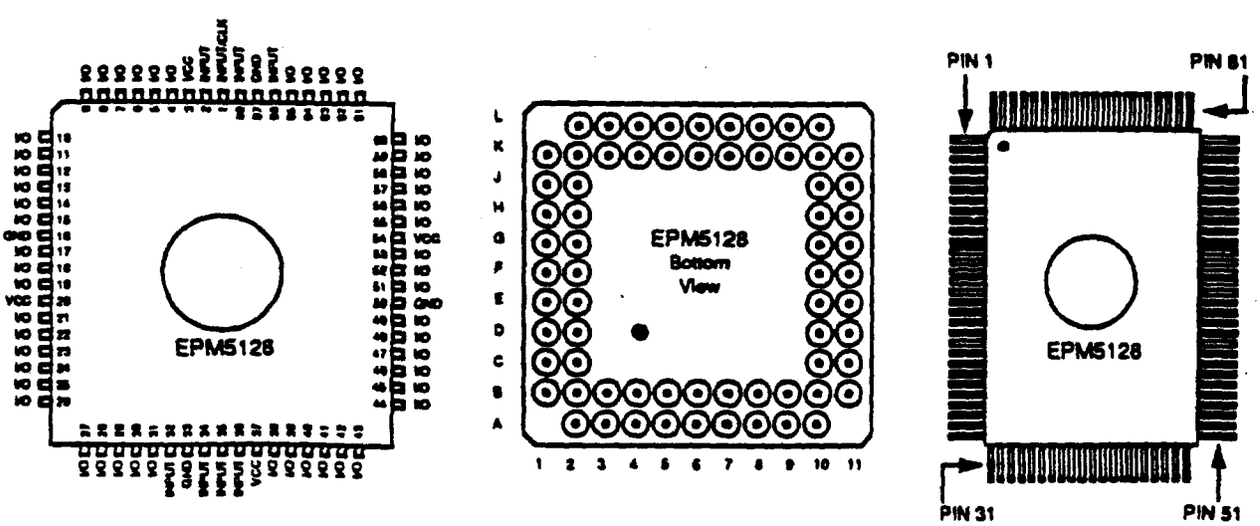
General Description

The Altera EPM5128 is a user-configurable, high-performance MAX EPLD that provides a high-density replacement for 7400-series SSI and MSI TTL and CMOS logic. (For example, a 74161 counter uses only 3% of the EPM5128.) The EPM5128 can replace over 60 TTL MSI and SSI components and integrate multiple 20- and 24-pin low-density PLDs. Figure 18 shows the J-lead and PGA package diagrams for the EPM5128.

3

Figure 18. EPM5128 Pin-Out Diagrams

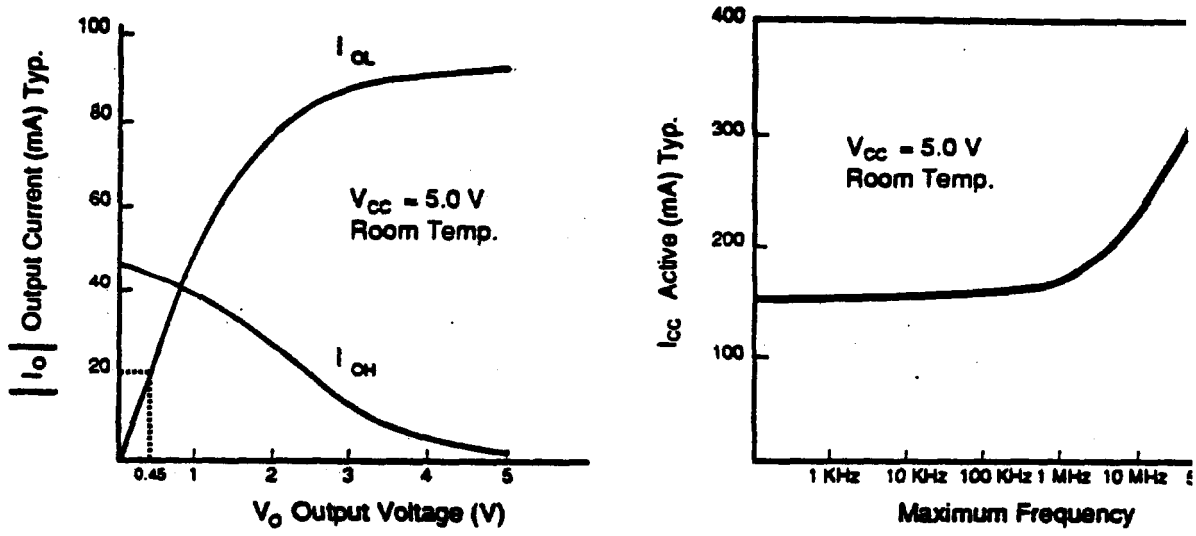
A quad flat pack (QFP) package is under development. Contact Altera Marketing for information. See Table 1 in this data sheet for PGA package pin-outs. Package outlines not drawn to scale.



J-Lead PGA QFP

Figure 19 shows output drive characteristics of EPM5128 I/O pin typical supply current versus frequency for the EPM5128.

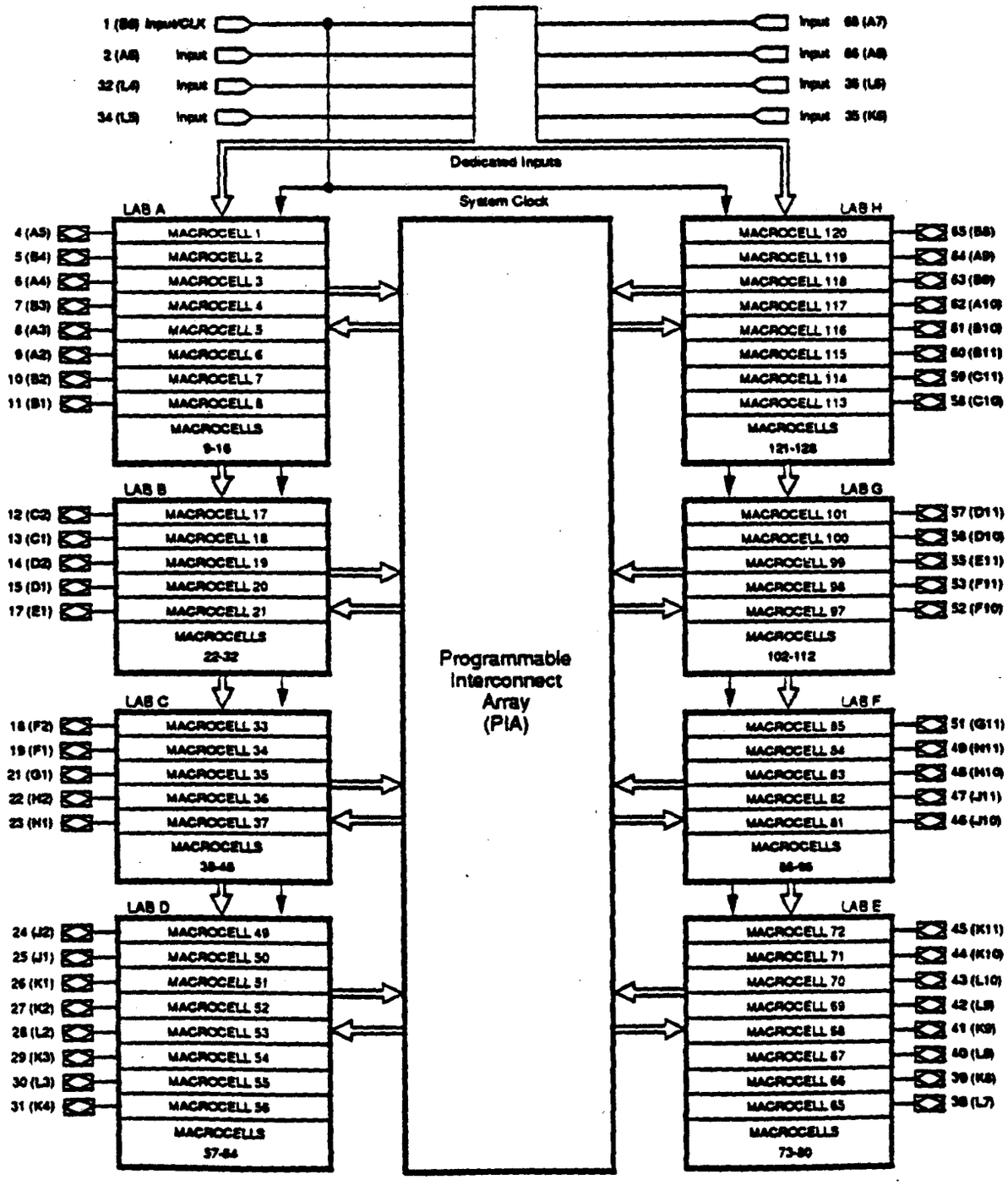
Figure 19. EPM5128 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5128 consists of 128 macrocells equally divided into 8 Logic A Blocks (LABs) that each contain 16 macrocells (see Figure 20). Each l also contains 32 expander product terms. The EPM5128 has 8 dedic input pins, one of which may be used as a synchronous system clock. EPM5128 contains 52 I/O pins that can be configured for input, outpu bidirectional data flow. Four of the LABs have 8 I/O pins, and the oth have 5 I/O pins.

Figure 20. EPM5128 Block Diagram

Numbers in parentheses are for PGA packages.



Absolute Maximum Ratings Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Ur
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	m
I_{OUT}	DC output current, per pin		–25	25	m
P_D	Power dissipation			2500	mV
T_{STG}	Storage temperature	No bias	–65	+150	°C
T_{AMB}	Ambient temperature	Under bias	–65	+135	°C
T_J	Junction temperature	Under bias		+150	°C

Recommended Operating Conditions *See Note (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	+70	°C
T_A	Operating temperature	For industrial use	–40	+85	
T_C	Case temperature	For military use	–55	+125	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *See Note (2), (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		+10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		+40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		150	225 (300)	mA
I_{CC3}	V_{CC} supply current	$V_I = V_{CC}$ or GND No load, f = 1.0 MHz *See Note (5)*		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Ma
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5128-1		EPM5128-2		EPM5128		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-reg. output	C1 = 35 pF		40		45		55	ns
t_{SU}	Setup time		15		20		25		ns
t_{H}	Hold time		0		0		0		ns
t_{CO1}	Clock to output delay	C1 = 35 pF		14		16		20	ns
t_{ASU}	Asynchronous setup time		5		6		8		ns
t_{AH}	Asynchronous hold time		6		8		10		ns
t_{CH}	Clock high time		8		10		12.5		ns
t_{CL}	Clock low time		8		10		12.5		ns
t_{ACH}	Asynchronous clock high time		11		14		16		ns
t_{ACL}	Asynchronous clock low time		9		11		14		ns
t_{ACO1}	Asynch. clock to output delay	C1 = 35 pF		25		30		35	ns
t_{CNT}	Minimum clock period			20		25		30	ns
f_{CNT}	Internal maximum frequency		50		40		33.3		MHz
t_{ACNT}	Minimum asynch. clock period	*See Note (6)*		20		25		30	ns
f_{ACNT}	Max. internal asynch. frequency	*See Note (6)*	50		40		33.3		MHz
f_{MAX}	Max. frequency; pipelined data		62.5		50		40		MHz

For information on internal timing parameters, refer to *App. Brief 75* (*EPM5000-Series MAX EPLD Timing*).

Internal Timing Parameters			EPM5128-1		EPM5128-2		EPM5128		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			5		7		9	ns
t_{IO}	I/O input pad and buffer delay			6		6		9	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		16	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		10		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		6		8		10		ns
t_{IC}	Clock delay			14		16		18	ns
t_{ICS}	System clock delay			2		2		3	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Progr. Interconn. Array delay			14		16		20	ns

3

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.

(2) Numbers in parentheses are for military and industrial temperature-range versions.

(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.

(4) V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.

(5) Measured with device programmed as a 16-bit counter in each LAB.

(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.

Product Availability

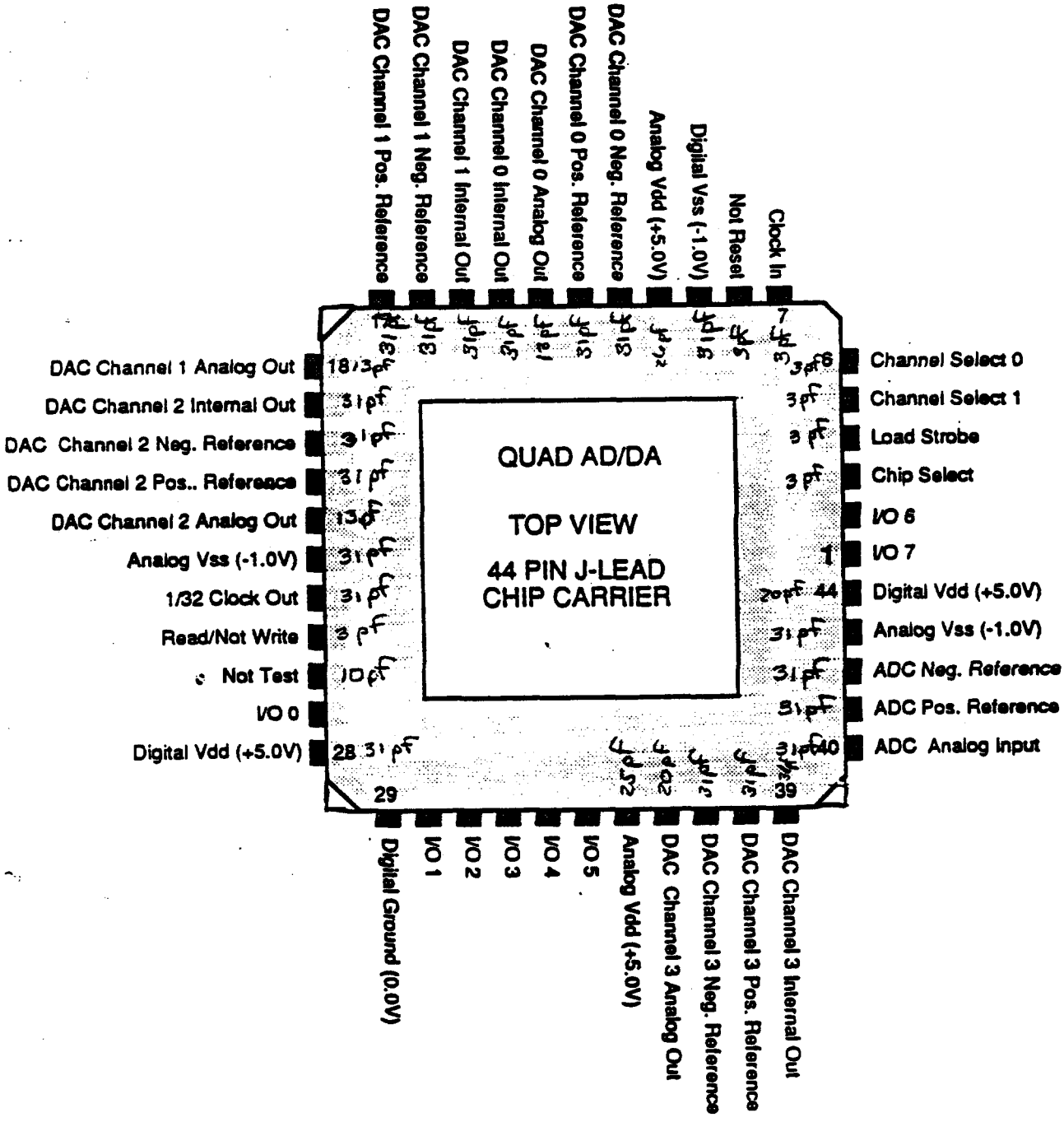
Grade		Availability
Commercial	(0° C to 70° C)	EPM5128-1, EPM5128-2, EPM5128
Industrial	(–40° C to 85° C)	EPM5128
Military	(–55° C to 125° C)	EPM5128

Note: Only military-temperature-range EPLDs are listed above. MIL-STD-883-compliant product specifications are provided in Military Product Drawings (MPDs), available from Altera Marketing by calling 1 (800) SOS-EPLD. These MPDs should be used to prepare Source Control Drawings (SCDs). See *Military Products* in this data book.

Table 1 shows the pin-outs for the EPM5128 PGA package.

Table 1. EPM5128 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B10	I/O	G1	I/O	K7	VCC
A3	I/O	B11	I/O	G2	VCC	K8	I/O
A4	I/O	C1	I/O	G10	GND	K9	I/O
A5	I/O	C2	I/O	G11	I/O	K10	I/O
A6	Input	C10	I/O	H1	I/O	K11	I/O
A7	Input	C11	I/O	H2	I/O	L2	I/O
A8	Input	D1	I/O	H10	I/O	L3	I/O
A9	I/O	D2	I/O	H11	I/O	L4	Input
A10	I/O	D10	I/O	J1	I/O	L5	Input
B1	I/O	D11	I/O	J2	I/O	L6	Input
B2	I/O	E1	I/O	J10	I/O	L7	I/O
B3	I/O	E2	GND	J11	I/O	L8	I/O
B4	I/O	E10	VCC	K1	I/O	L9	I/O
B5	VCC	E11	I/O	K2	I/O	L10	I/O
B6	Input/CLK	F1	I/O	K3	I/O		
B7	GND	F2	I/O	K4	I/O		
B8	I/O	F10	I/O	K5	GND		
B9	I/O	F11	I/O	K6	Input		


QUAD AD/DA
TOP VIEW
44 PIN J-LEAD
CHIP CARRIER
DAC Channel 1 Analog Out
DAC Channel 2 Internal Out
DAC Channel 2 Neg. Reference
DAC Channel 2 Pos.. Reference
DAC Channel 2 Analog Out
Analog Vss (-1.0V)
1/32 Clock Out
Read/Not Write
Not Test
I/O 0
Digital Vdd (+5.0V)
Digital Ground (0.0V)
I/O 1
I/O 2
I/O 3
I/O 4
I/O 5
Analog Vdd (+5.0V)
DAC Channel 3 Analog Out
DAC Channel 3 Neg. Reference
DAC Channel 3 Pos. Reference
DAC Channel 3 Internal Out
ADC Analog Input
ADC Pos. Reference
ADC Neg. Reference
Analog Vss (-1.0V)
Digital Vdd (+5.0V)
I/O 7
I/O 6
Chip Select
Load Strobe
Channel Select 1
Channel Select 0
Clock In
Not Reset
Digital Vss (-1.0V)
Analog Vdd (+5.0V)
DAC Channel 0 Neg. Reference
DAC Channel 0 Pos. Reference
DAC Channel 0 Analog Out
DAC Channel 0 Internal Out
DAC Channel 1 Internal Out
DAC Channel 1 Neg. Reference
DAC Channel 1 Pos. Reference

15 devices

9/21/89

TESTED ASIC FOR MIN/MAX Power Supply Currents. The 4 DACs were SET to Full scale (2.56V out) and were then loaded for a 1 LSB change (2.55V @ 17.5mA) and the power supply currents were then recorded.

	MIN (NO LOAD)	MAX	
+5V	27mA	77mA ±5mA	(SOURCING)
-1.0V	2.5 mA	26mA	(SINKING)
+2.56V	3.5mA	3.5mA	(SOURCING)

The Power Supplies were monitored for noise and Glitches — none were observed.

The above currents are the avg MIN/MAX currents of the US2 D/A A/D chips available.

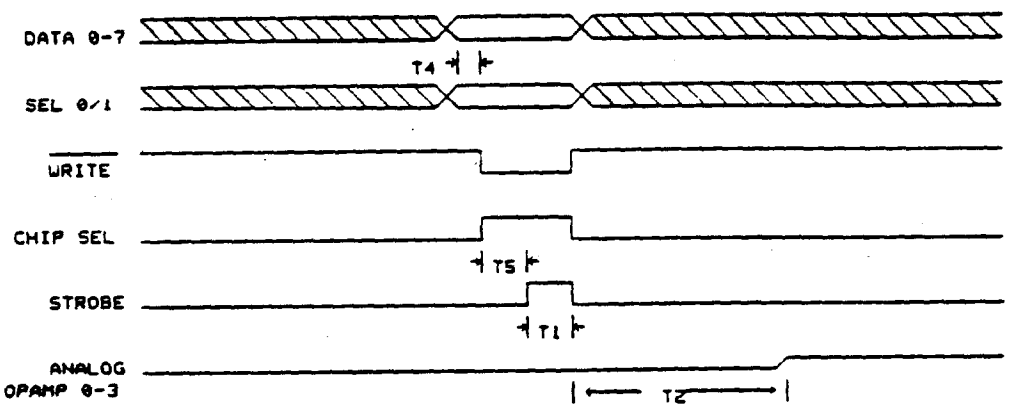
Z_{OUT} 3.0 – 14Ω / OUTPUT

P.S. currents

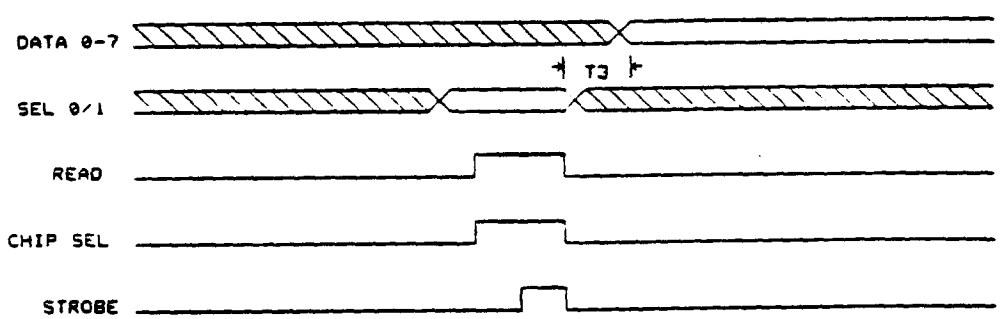
		USE
64 x 3.5mA	224mA	250
64 x 2.5mA	160mA	200
64 x 27	1,728mA	2A

WE CAN DRIVE ENTIRE BOARD WITH 2 PACKAGE

TYPICAL WRITE CYCLE



TYPICAL READ CYCLE



TIMING*

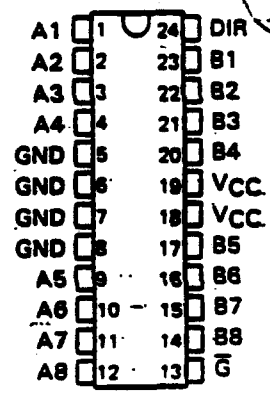
T1 = 100nS MIN
T2 = 3.25uS MAX
T3 = 40nS MAX
T4 = 4nS MIN
T5 = 100nS MIN

* APPROXIMATE VALUES FROM SIMULATION/DATA SHEETS

D2967, JULY 1987–REVISED AUGUST 1988

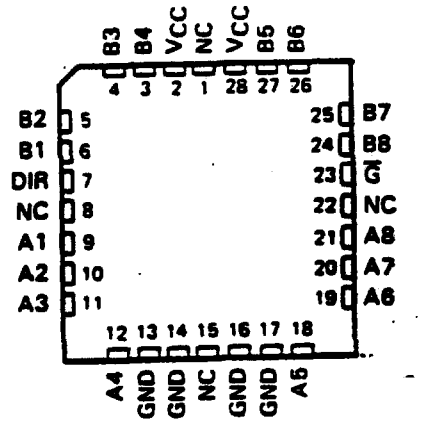
- 3-State Outputs Drive Bus Lines Directly
- Inputs are TTL-Voltage Compatible
- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11245 . . . JT PACKAGE
74ACT11245 . . . DW OR NT PACKAGE
(TOP VIEW)



SMT
Small outline
1/34
100

54ACT11245 . . . FK PACKAGE
(TOP VIEW)



NC = No internal connection

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus, or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The 54ACT11245 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74ACT11245 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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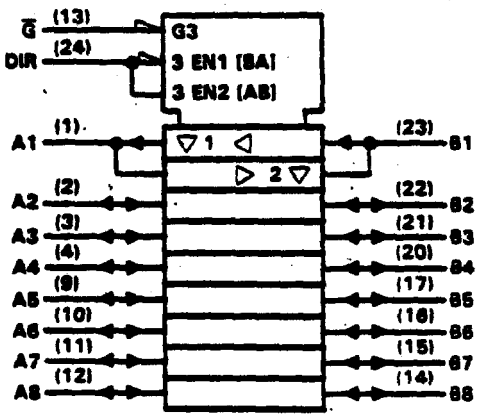
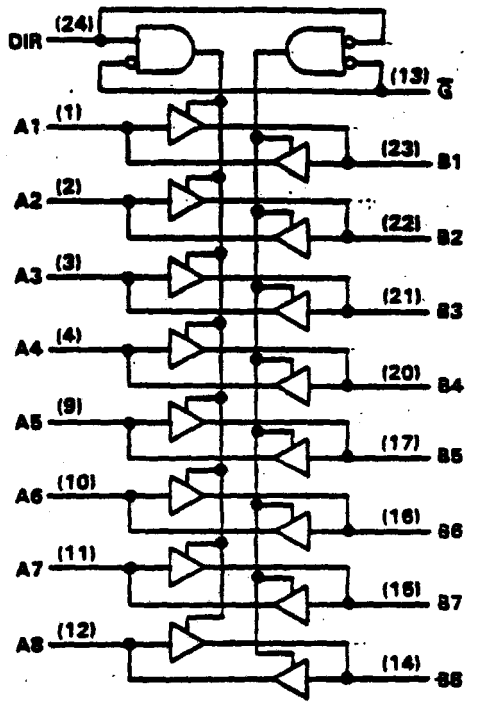
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC}+0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

		54ACT11245		74ACT11245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	0	10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11245		74ACT11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 µA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	µA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	µA
ΔI_{CC}‡	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_{io}	V_{IO} = V_{CC} or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

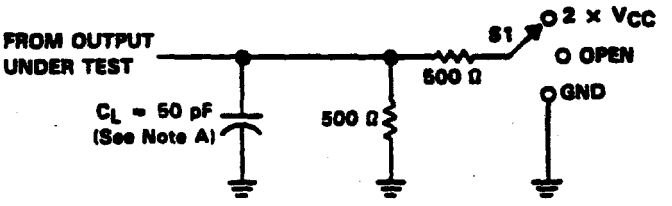
switching characteristics, V_{CC} = 5 V ±0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11245		74ACT11245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	6.2	9.2	1.5	10.6	1.5	10	ns
t_{PHL}			1.5	5.4	8.6	1.5	9.6	1.5	9.1	
t_{PZH}	$\overline{G}$	A or B	1.5	8.1	12	1.5	14.1	1.5	13.2	
t_{PZL}			1.5	8.2	11.7	1.5	13.7	1.5	12.9	
t_{PHZ}	$\overline{G}$	A or B	1.5	9.3	11.8	1.5	13.6	1.5	12.9	
t_{PLZ}			1.5	9.8	12.9	1.5	14.6	1.5	13.9	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

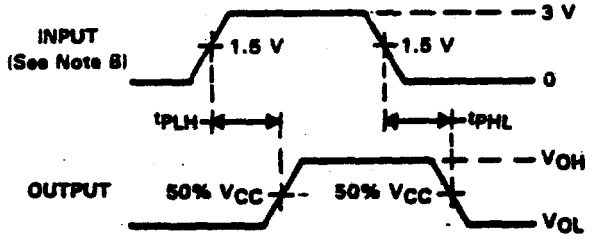
PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	88	pF
		Outputs disabled		19	

PARAMETER MEASUREMENT INFORMATION

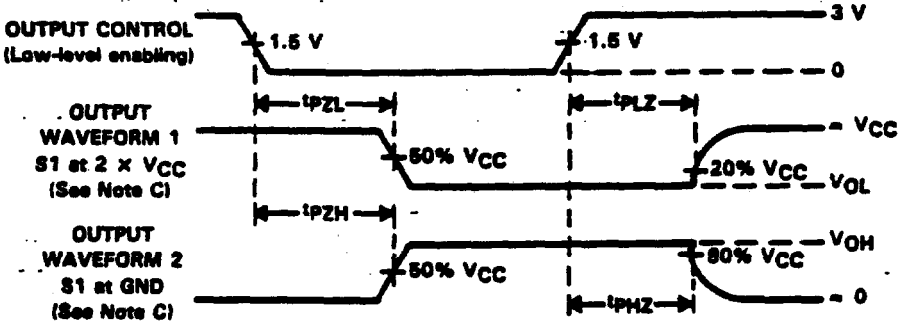


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

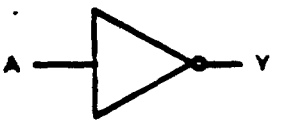
These devices contain six independent inverters.

The SN5404, SN54H04, SN54L04, SN54LS04 and SN54S04 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7404, SN74H04, SN74LS04 and SN74S04 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each inverter)

INPUTS A	OUTPUT Y
H	L
L	H

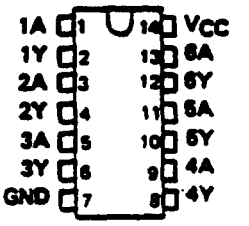
logic diagram (each inverter)



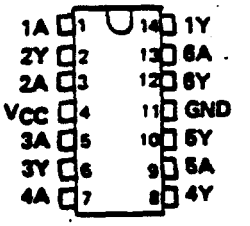
positive logic

$$Y = \overline{A}$$

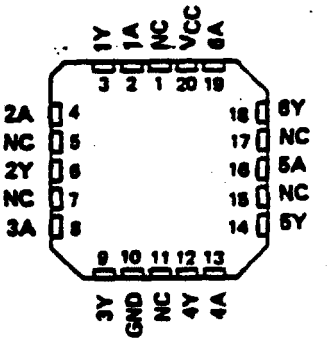
SN5404, SN54H04, SN54L04 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74H04 . . . J OR N PACKAGE
SN74LS04, SN74S04 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5404, SN54H04 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
SN74LS04, SN74S04 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

National Semiconductor

LM111/LM211/LM311 Voltage Comparator

General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

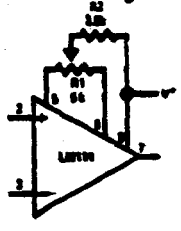
The LM211 is identical to the LM111, except that its performance is specified over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C.

Features

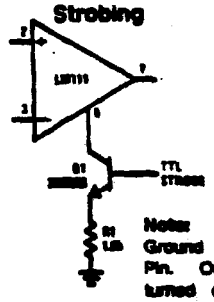
- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Typical Applications**

Offset Balancing



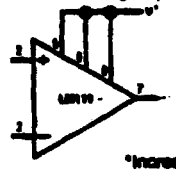
Strobing



Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

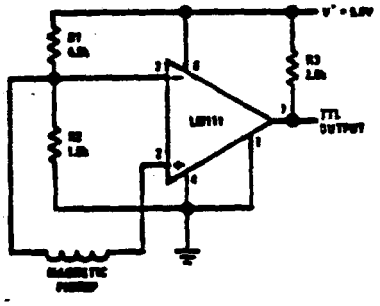
**Note: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

Increasing Input Stage Current*

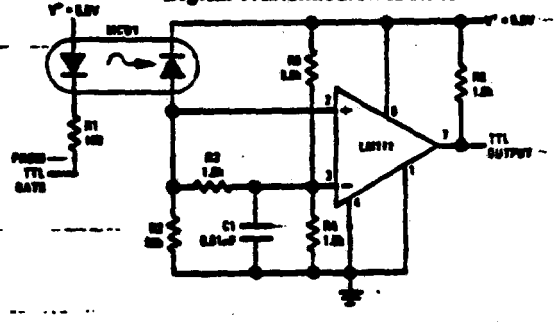


*Increases typical common-mode slew from 7.0V/μs to 18V/μs.

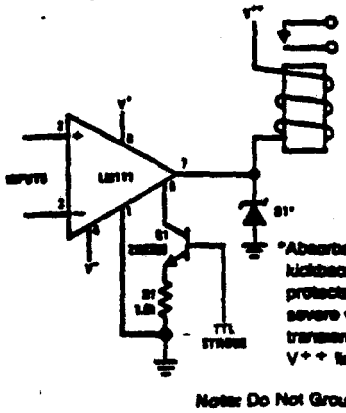
Detector for Magnetic Transducer



Digital Transmission Isolator



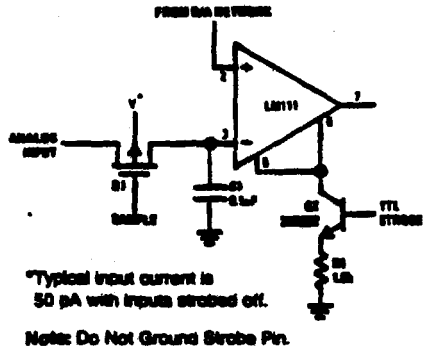
Relay Driver with Strobe



*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

Note: Do Not Ground Strobe Pin.

Strobing off Both Input* and Output Stages



*Typical input current is 50 pA with inputs strobed off.

Note: Do Not Ground Strobe Pin.

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5

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Absolute Maximum Ratings for the LM111/LM211

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec

Operating Temperature Range LM111	−55°C to 125°C
LM211	−25°C to 85°C
Storage Temperature Range	−65°C to 15
Lead Temperature (Soldering, 10 sec)	260°C
Voltage at Strobe Pin	V+ −5V
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Rating (Note 8)	300V

Electrical Characteristics for the LM111 and LM211 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current (Note 6)	$T_A = 25°C$	2.0	3.0	5.0	mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50$ k			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range	$V^+ = 15V$, $V^- = -15V$, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,-14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{OUT} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 110°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe to ground; it should be current driven at 3 to 5 mA.

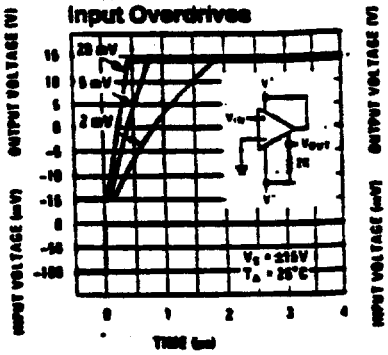
Note 7: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

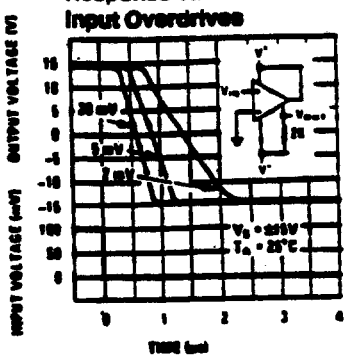
(21)

LM311 Typical Performance Characteristics (Continued)

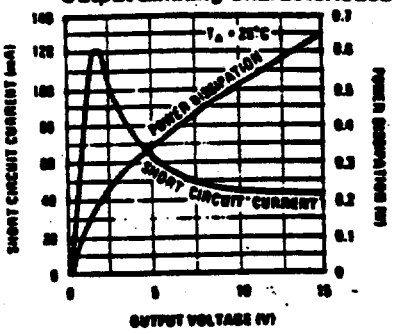
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



Output Limiting Characteristics



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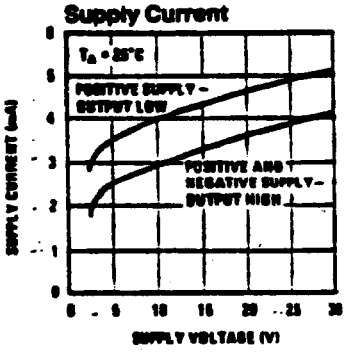
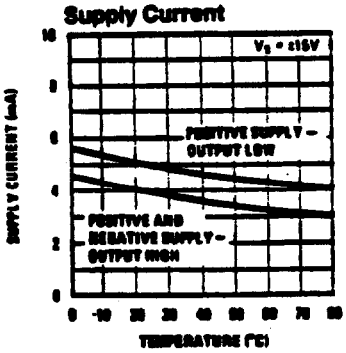
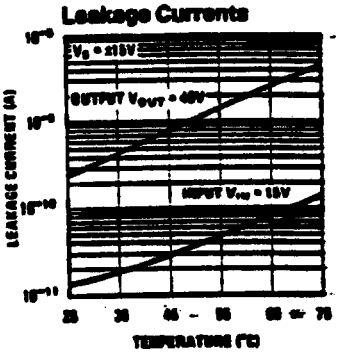
Supply Current



Supply Current



Leakage Currents



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(21)

Absolute Maximum Ratings for the LM311

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage V_{74})	40V
Ground to Negative Supply Voltage V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
ESD Rating (Note 7)	300V
Output Short Circuit Duration	10 sec
Operating Temperature Range	0° to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	260°C
Voltage at Strobe Pin	$V^+ - 5V$
Soldering Information	
Dual-in-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics for the LM311 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$	1.5	3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA $V^- = V_{GRND} = -5V$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50K$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8, −14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{OUT} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and the Ground pin at ground, and $0°C < T_A < +70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 7: Human body model, 1.5 kΩ in series with 100 pF.